Low Noise / High Resolution DAC II

Physics Basel SP 1060

Commander Description | Revision 1.2

For Software Release 3.4.9

Michael Steinacher | October 2022

University of Basel

1 Used Abbreviations

The Following abbreviations are used in this manual:
LNHR = Low Noise / High Resolution
DAC = Digital/Analog Converter
LED = Light Emitting Diode
BNC = Bayonet Nut Connector
AWG = Arbitrary Waveform Generator
WAV = Wave
WF = Waveform
RMP = Ramp
LBW = Low Bandwidth (100 Hz)
HBW = High Bandwidth (100 kHz)
SWG = Standard Waveform Generation
POLY = Polynomial
2D = Two-Dimensional
HEX = Hexadecimal
LAN = Local Area Network
NIC = Network Interface Card
msec = milli-second (1E-3)
µsec = micro-second (1E-6)
NaN = Not a Number
Inf = Infinite
Float = Floating-point number
ppm = Parts per million (1E-6)
AGND = Analog Ground
INL = Integral Nonlinearity
FFT = Fast Fourier Transformation
RMS = Root Mean Square (Effective Value)
DAQ = Data Acquisition

2 Overview

The "LNHR DAC II Commander" is a PC-Windows application to control and setup the LNHR DAC II. The "Commander" runs on a 64-bit Microsoft Windows 10 PC with minimum 8 Giga Byte of RAM. The bidirectional communication between the device and the PC is performed via a Gigabit Ethernet LAN connection - see chapter "Network Connection".
- see chapter "Installing the LNHR DAC II Commander"

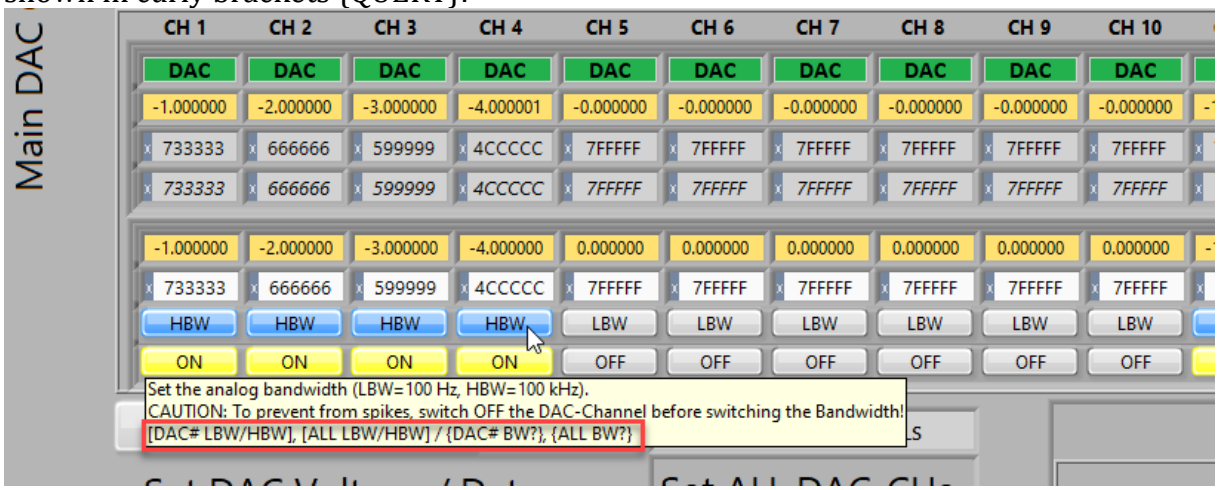
This description applies to the application "LNHR DAC II Commander" Revision 3.4.9 connected to a LNHR DAC II (SP 1060) with 24 DAC-Channels and with a Software Release of 3.4.9 – you can easily check the installed release on the local LCD under the menu item "Software Release".

Two different version of the LNHR DAC II are available:
The fully equipped 24 DAC-Channels version and the 12 DAC-Channels version which has only one DAC-Board (Lower DAC-Board) with the DAC-Channels 1 to 12. Since all other components are the same (including the front-panel) the 12 DAC-Channels version can later be upgraded to a 24 DAC-Channels version; for this upgrade the device has to be returned to the producer (Physics Basel).

This “Commander Description” documents the fully equipped 24 DAC-Channels version. For the 12 DAC-Channels version some options and numbers are different than indicated in this manual, since the Higher DAC-Board with the DAC-Channels 13 to 24 are missing.

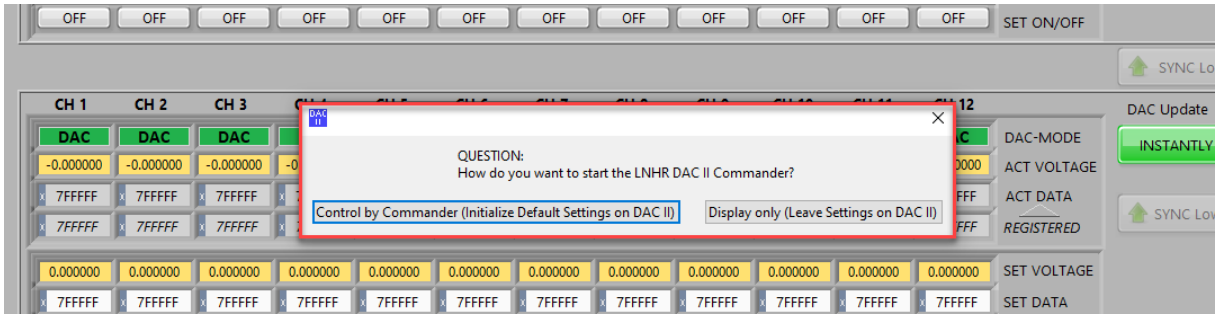
Nevertheless, this “LNHR DAC II Commander” application can control 12 or 24 DAC-Channels versions without any modifications. The version (12 or 24 DAC-Channels) of the connected LNHR DAC II gets automatically detected. When controlling a 12 DAC-Channels version the not available controls and indicators get automatically disabled and greyed out. Also, the range of selectable DAC-Channels is automatically adjusted.

While operating with the LNHR DAC II Commander the last line of the “Tip Strip” (which pops up when the mouse is on a control or indicator) shows the corresponding remote command string as a hint.
SET Commands are indicated in square brackets [SET] while QUERY Commands are shown in curly brackets {QUERY}:



For further information see the “LNHR DAC II Programmer’s Manual” and also the “LNHR DAC II User’s Manual”.

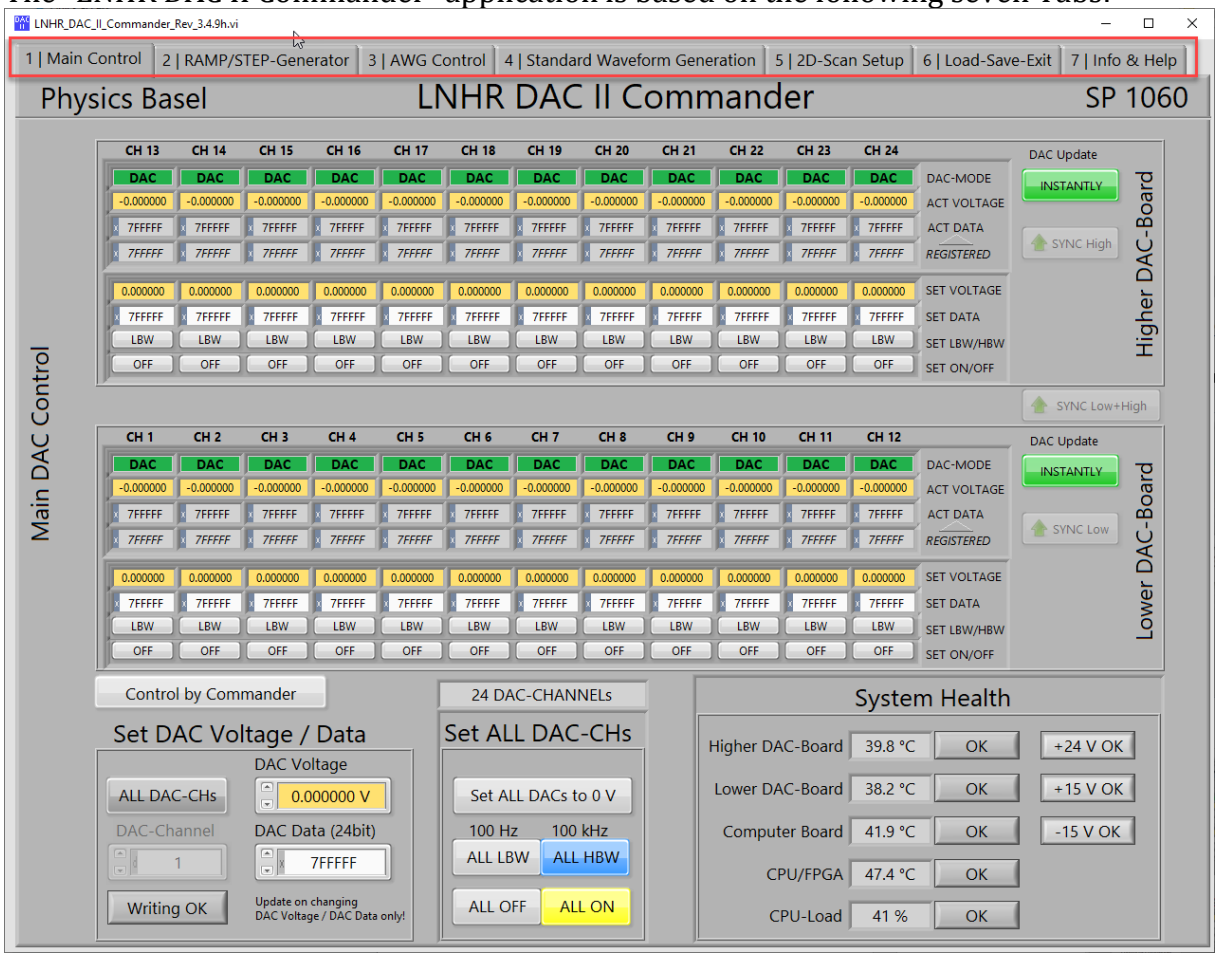
When the “LNHR DAC II Commander” is started, the user is asked in which mode he wants to start the application. When selecting “Control by Commander” all the controls are initialized to their default values; for example, all DAC-Channels are switched OFF. When selecting “Display only” no default settings are written from the Commander to the device. The actual settings and states of LNHR DAC II are kept and they are displayed only; all controls are disabled.



Later on, one can still alter the mode between “Control by Commander” and “Display only”.

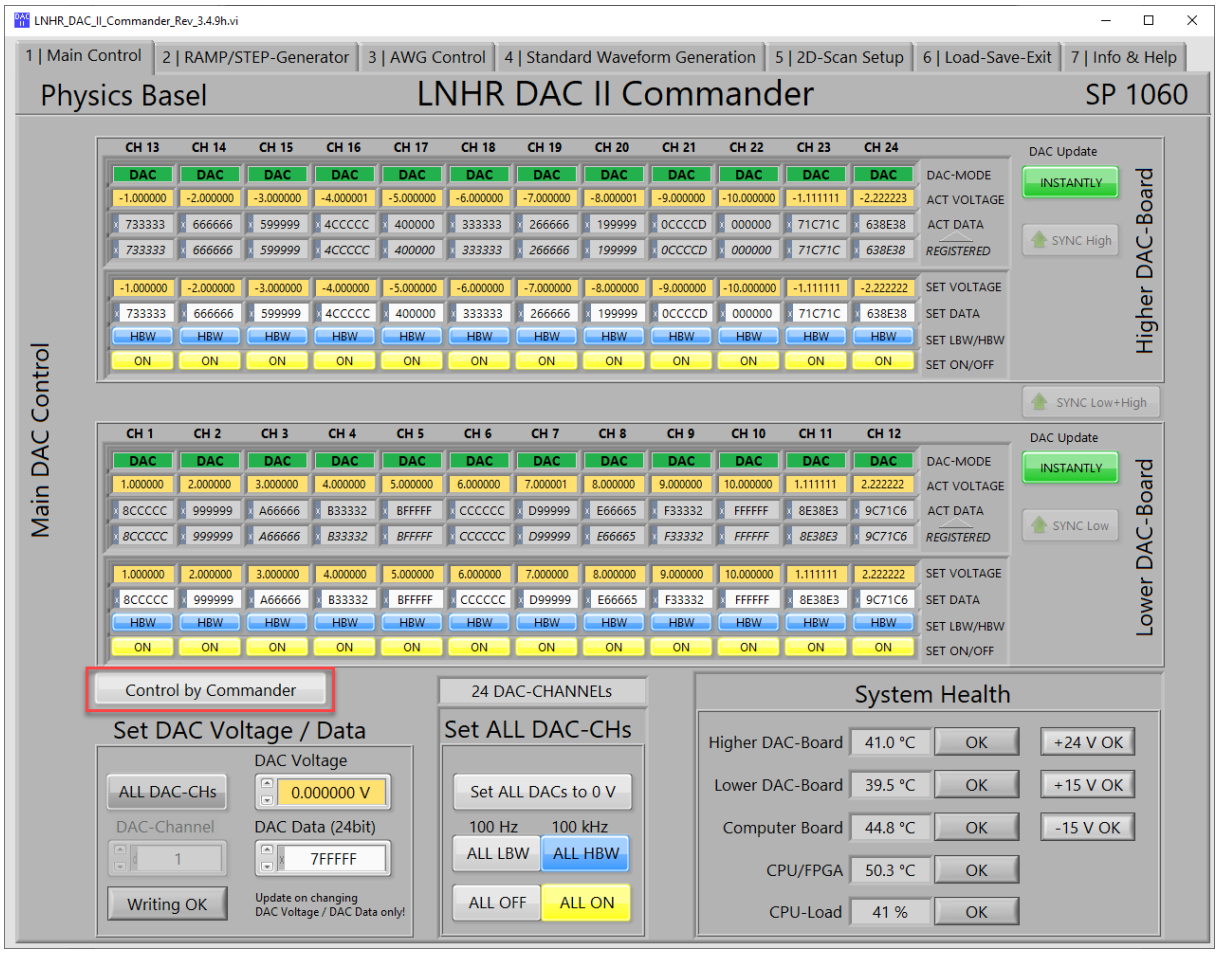
3 Description of the Tabs

The “LNHR DAC II Commander” application is based on the following seven Tabs:



1. **Main Control**
   Displays the status of the device and allows to set the individual DAC voltages and control its output stage including the synchronization.
2. **RAMP/STEP-Generator**
   Controls the four RAMP/STEP-Generators and set its parameters. The settings for the (adaptive) 2D-Scan are also done here.
3. **AWG Control**
   Controls the four AWGs and set its parameters. Further the AWG-Memories can be readout here.
4. **Standard Waveform Generation**
   Generates or Loads the Waveforms for the four AWGs. Saves the generated Waveforms to a text-file on the PC.
5. **2D-Scan Setup**
   The four different 2D-Scans are defined and build here. Further the 2D-Scans can be controlled (Start/Stop) and monitored.
6. **Load-Save-Exit**
   Loads and Saves the Settings of the Commander controls. Exit the Commander with updating the location of the folders for the Settings, the Waveforms and the PDF-Manuals.
7. **Info & Help**
   Shows the System Information and allows access to the PDF-Manuals. Further the Linearization Coefficients of all DAC-Channels are displayed here.

4 Tab 1 | Main Control

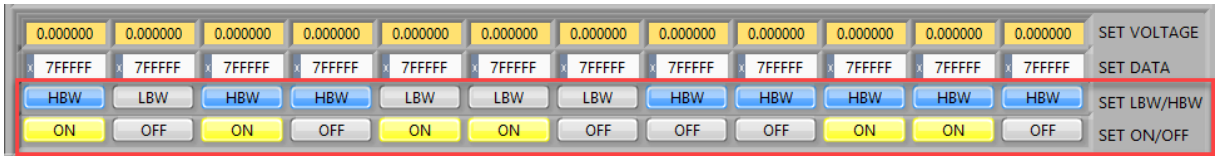


If “Control by Commander” is selected, all controls on all Tabs are enabled.

The “Main Control Tab” shows the status-overview of the device on a single page. On top the “Higher DAC-Board” with the DAC-Channels 13…24 is shown and below the “Lower DAC-Board” with the DAC-Channels 1…12. On the bottom right the “System Health” shows the temperatures, the status of the supply voltages and the CPU-Load.

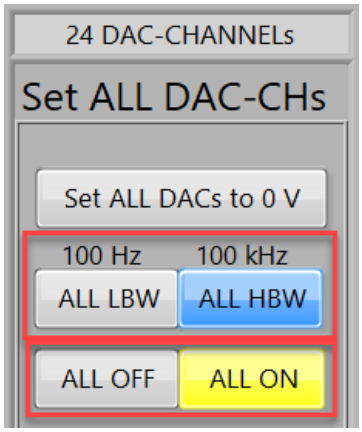
In the middle bottom part “Set ALL DAC-CHs” all DAC Voltages can be set to zero (0 V), all DAC-Channels can be switched ON/OFF and set to LBW (100 Hz) or HBW (100 kHz). In the left bottom section “Set DAC Voltage / Data” the DAC Voltage or the DAC Data (24bit) of a single DAC-Channel or ALL DAC-Channels can be modified.

4.1 Select ON/OFF and LWB/HBW



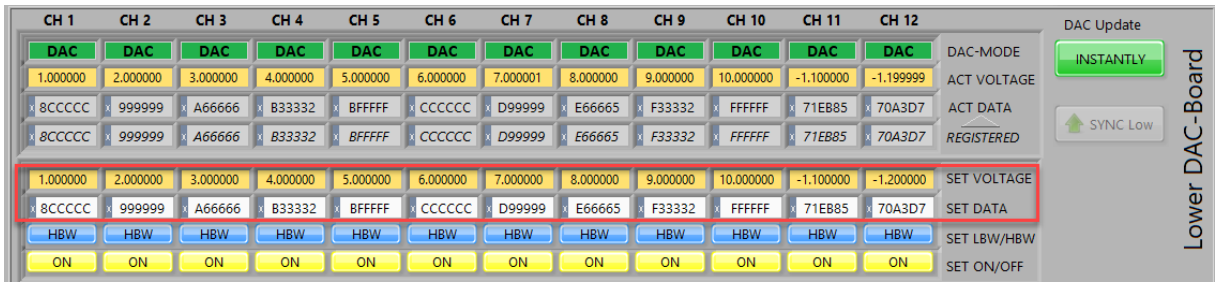
In the field “SET ON/OFF” the DAC-Channels can be switched ON/OFF and in the field “SET LBW/HBW” the Bandwidth can be changed between LBW=100 Hz and HBW=100 kHz. You can toggle between ON/OFF and LBW/HBW by clicking on the corresponding button.

By using the selection "Set ALL DAC-CHs" all DAC-Channels can be switched ON/OFF and all Bandwidths can be altered between LBW and HBW:



CAUTION: When switching the Bandwidth, glitch-voltages can occur on the DAC output! Therefore, it is strongly recommended to switch OFF the corresponding DAC-Channel before changing its Bandwidth. After switching the Bandwidth, wait at least for 0.5 sec before switch ON the DAC-Channel again. When doing so, the Bandwidth can be changed safely and glitch-free.

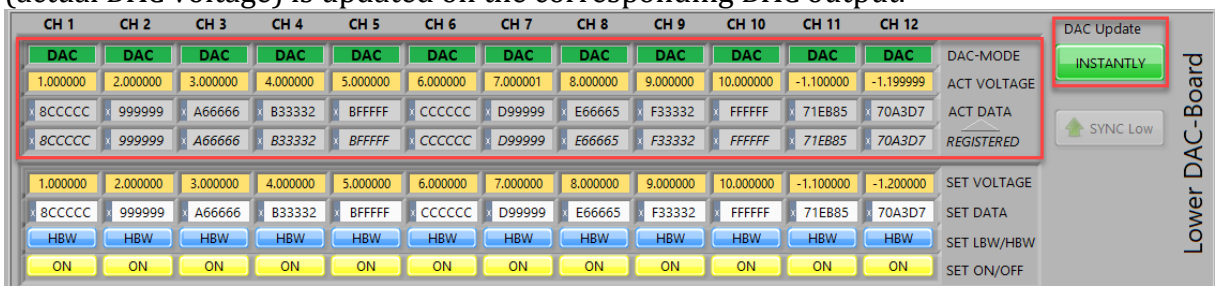
4.2 Set DAC Voltage / Data



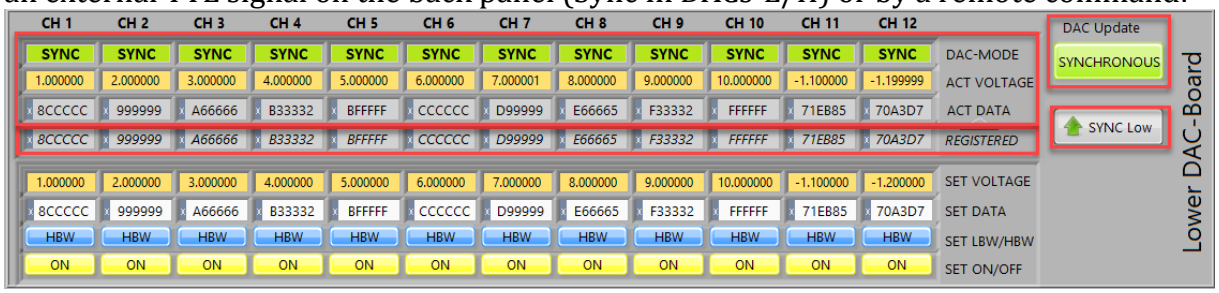
The DAC voltage can be set by editing either the "SET VOLTAGE" control field or the "SET DATA" control field. When editing the "SET VOLTAGE" control field, the "SET DATA" control field is automatically updated and vice versa; see chapter "Converting DAC-Voltage to DAC-Value".

Note: After editing a value in a control-field, press ENTER or leave this control-field with the mouse-curser. Otherwise, the value is NOT updated.

The "SET DATA" gets copied to the "*REGISTERED*" DAC Data. When the DAC Update mode is "INSTANTLY" (all DAC-Channels in "DAC" mode) the "*REGISTERED*" DAC Data are immediately transferred to the "ACT DATA" (actual DAC Data). Then the "ACT VOLTAGE" (actual DAC voltage) is updated on the corresponding DAC output.

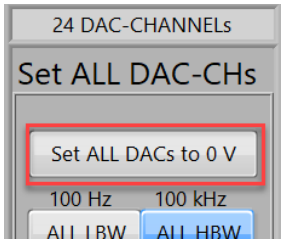


When the DAC Update mode is "SYNCHRONOUS" (DAC-Channels in "SYNC" mode) the "*REGISTERED*" DAC Data are transferred to the "ACT DATA" (actual DAC Data) on a SYNC-event. Such a SYNC-event can be released by pressing the button "SYNC Low/High" or by an external TTL signal on the back panel (Sync In DACs-L/H) or by a remote command:

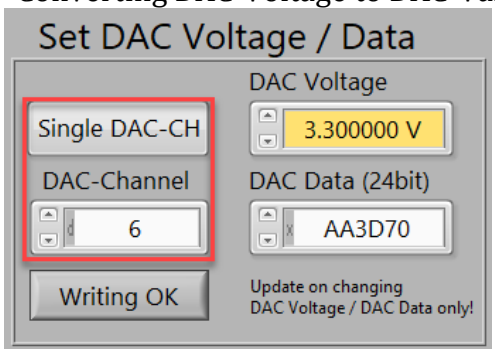


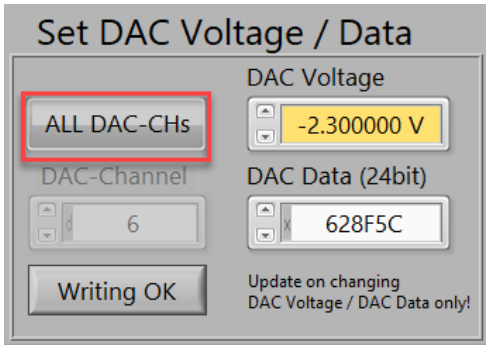
Then all "ACT VOLTAGEs" (actual DAC voltages) on one DAC-Board (Low or High) are synchronously updated on this SYNC-event.

With the button "Set ALL DACs to 0 V" all "SET VOLTAGEs" can be set to zero (0 V).



By using the selection "Set DAC Voltage / Data" a Single DAC-Channel or ALL DAC-Channels can be set to a "DAC Voltage" or a "DAC Data (24 bit)" – note, that only the "SET VOLTAGE / DATA" is updated. When editing the "DAC Voltage" control field, the "DAC DATA (24 bit)" control field is automatically updated and vice versa; see chapter "Converting DAC-Voltage to DAC-Value".

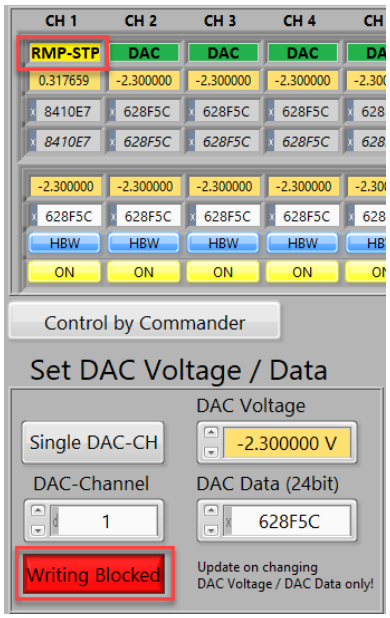




An update is only made on a changing input value in one of the two control fields "DAC Voltage" or "DAC Data (24 bit)".

Note: After editing a value in a control-field, press ENTER or leave this control-field with the mouse-curser. Otherwise, the value is NOT updated.

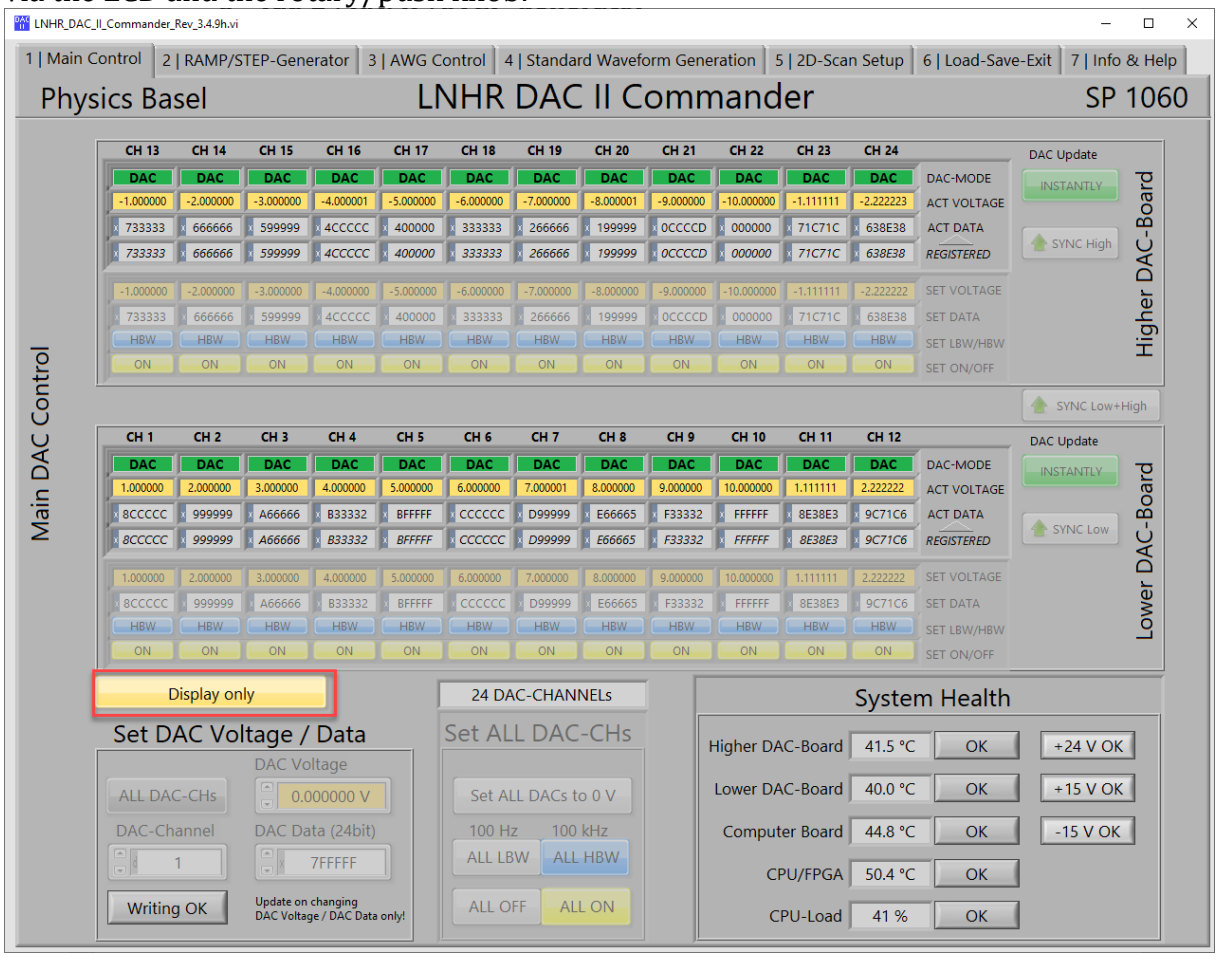
The indicator "Writing OK" is set when the corresponding DAC-Channel is in "DAC" or in "SYNC" mode. When trying to write to a DAC-Channel which is occupied by a RAMP/STEP-Generator (RMP-STP) or by an AWG Function (AWG) the "Writing Blocked" is displayed:



In this example, the DAC-Channel 1 is already occupied by a running RAMP/STEP-Generator (RMP-STP) and therefore the writing is blocked.

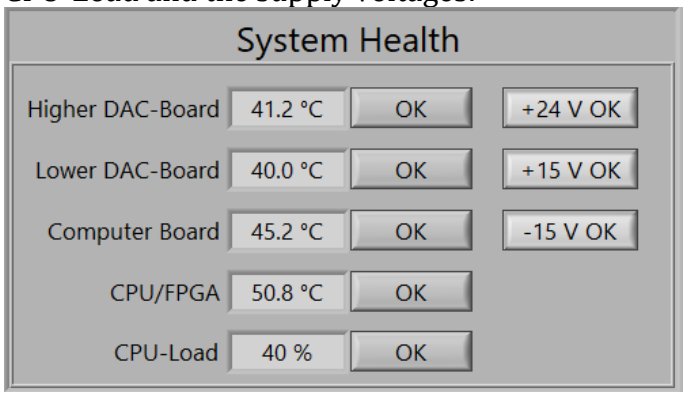
4.3 Set “Display only”

When “Display only” is selected, all controls on all the Tabs are disabled and greyed out. In this mode the “LNHR DAC II Commander” monitors only and no values can be modified by the user. Nevertheless, the device can be controlled via remote commands or locally via the LCD and the rotary/push knob:



4.4 System Health

The window “System Health” gives an overview of the LNHR DAC II temperatures, the CPU-Load and the supply voltages:



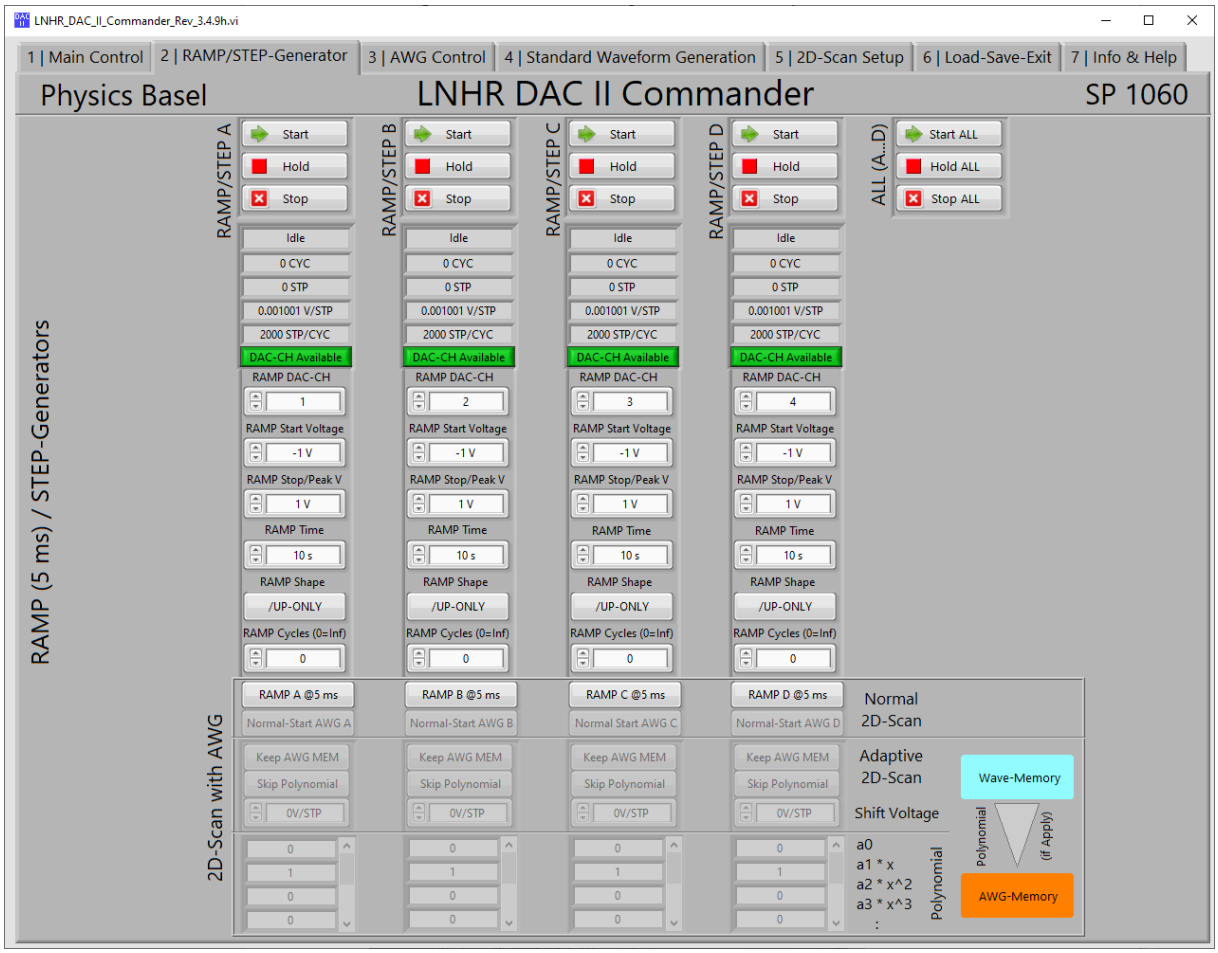
The Temperatures of the two “DAC-Boards” and the “Computer Board” must be below 70°C to be “OK”; the Temperature of the “CPU/FPGA” must be below 90°C to be “OK”.

Note: A running AWG disables the temperature measurement on the corresponding DAC-Board (Lower/Higher DAC-Board); then the temperature is displayed with “NaN°C”.

A CPU-Load smaller than 95% it is “OK”; for a CPU-Loads >95% the system gets overloaded the number of parallel running RAMP/STEP-Generators must deceased.

The three supply voltages (+24 V, +15 V and -15 V) are monitored and if one of them is LOW, all DAC-Channels are immediately switched OFF.

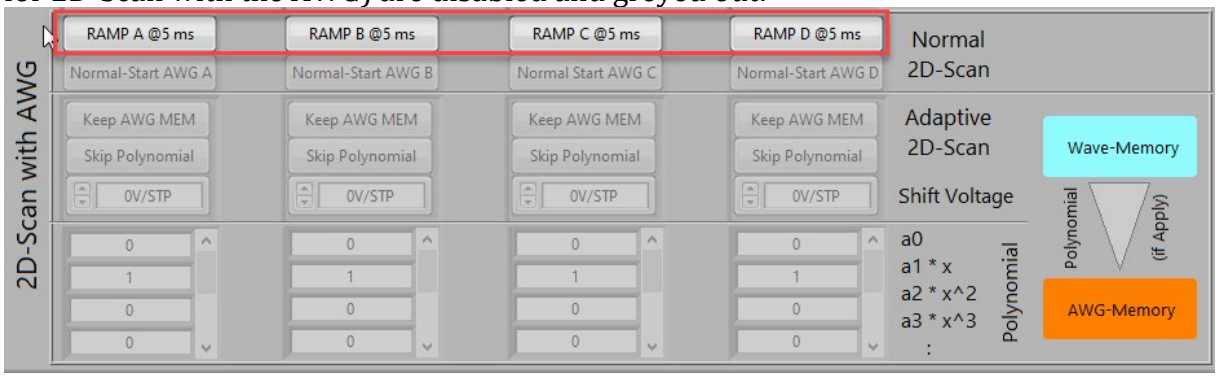
5 Tab 2 | RAMP/STEP-Generator



The parameters and the modes of the four individual RAMP/STEP-Generators (A, B, C, D) can be set on this Tab. Further the RAMP/STEP-Generators can be start, hold and stop here.

5.1 Select RAMP Mode

If a normal RAMP voltage should be performed, the corresponding button "RAMP A/B/C/D @5 ms" must be selected; then the parameters for the STEP-Generator (needed for 2D-Scan with the AWG) are disabled and greyed out:

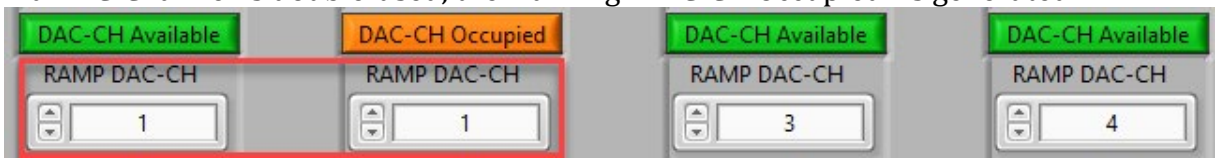


In the RAMP Mode, a user-defined voltage RAMP is generated with a fixed DAC update period of 5 msec; this means that every 5 msec the voltage of a running RAMP is updated. For the description of the STEP-Generator function see the chapter "Select STEP Mode".

5.2 Select RAMP DAC-Channels

The user can define the DAC-Channel on which to output the corresponding RAMP-Generator. If the selected "RAMP DAC-CH" is available (not used by another RAMP or AWG) the indicator "DAC-CH Available" is green:

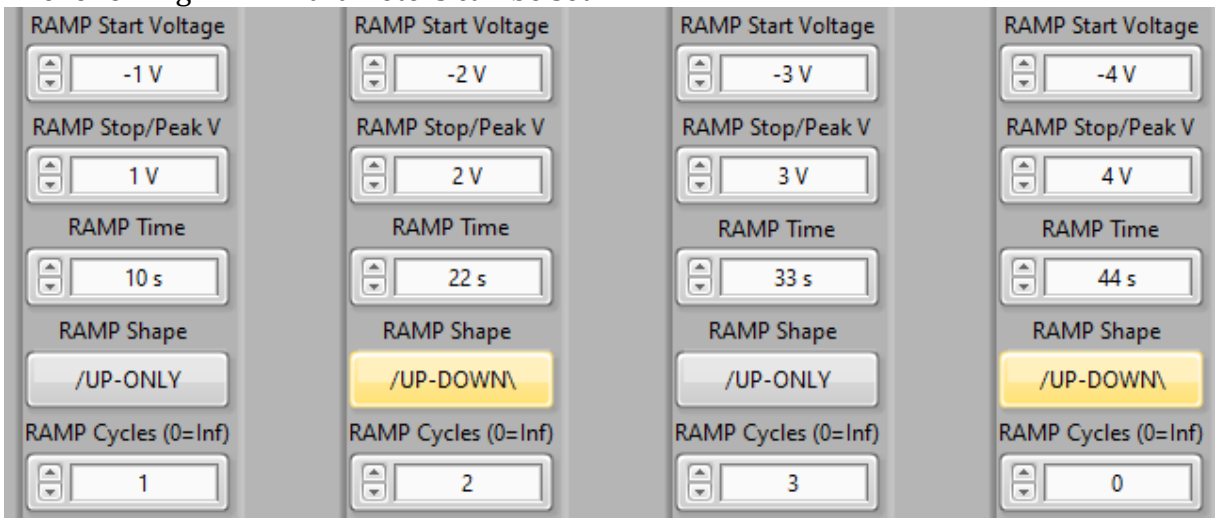
If a DAC-Channel is double-used, the warning "DAC-CH Occupied" is generated:



Note: On a running RAMP-Generator the flag "DAC-CH Occupied" is displayed and the "RAMP DAC-CH" and all the RAMP Parameters are disabled and greyed out.

5.3 Set RAMP Parameters

The following RAMP Parameters can be set:

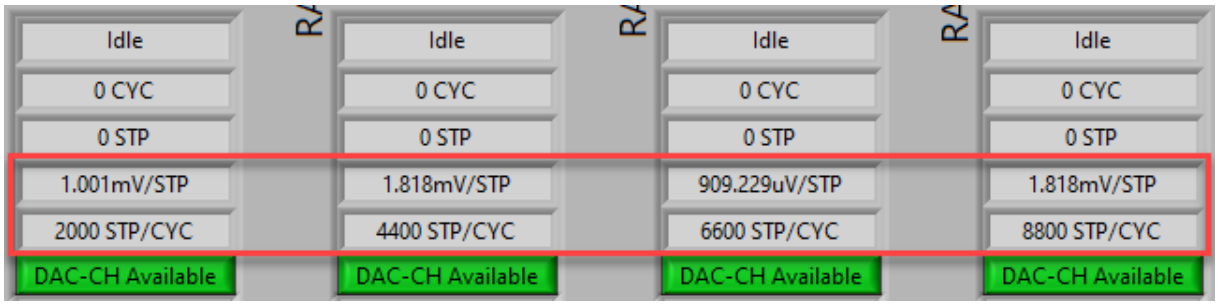


"RAMP Start Voltage": Voltage where the RAMP starts.
"RAMP Stop/Peak Voltage": Voltage where the RAMP stops or peaks.
"RAMP Time": Duration of one RAMP cycle.
"RAMP Shape": "/UP-ONLY" is a sawtooth RAMP, "/UP-DOWN\" is a triangle RAMP.
"RAMP Cycles (0=Inf)": Number of RAMP cycles; at zero, the RAMP repeats indefinitely.

When a triangle RAMP ("/UP-DOWN\") is selected, the voltage ramps from the "RAMP Start Voltage" up to the "RAMP Stop/Peak Voltage" and the back to the "RAMP Start Voltage"; this is one complete RAMP cycle.

When a sawtooth RAMP ("/UP-ONLY") is selected, the voltage ramps only up to the "RAMP Stop/Peak Voltage"; this is one complete RAMP cycle.

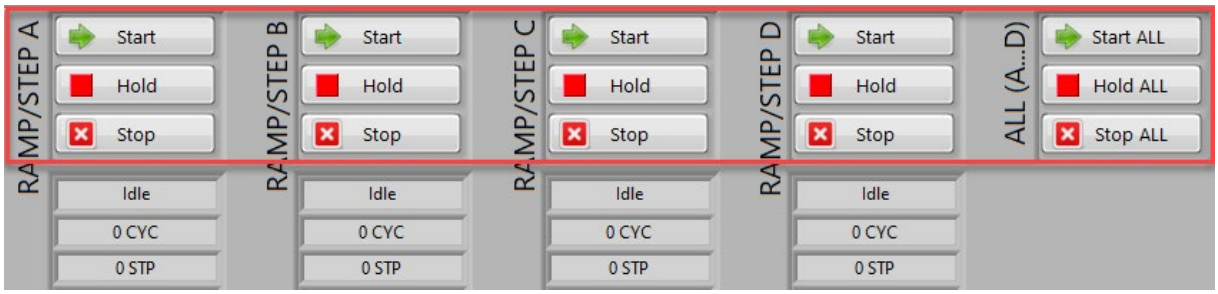
From the RAMP Parameters above the "Step-Size [V/STP]" and the "Number of Steps per Cycle [STP/CYC]" are calculated:



With these values, the user can verify that reasonable RAMP Parameters have been chosen.

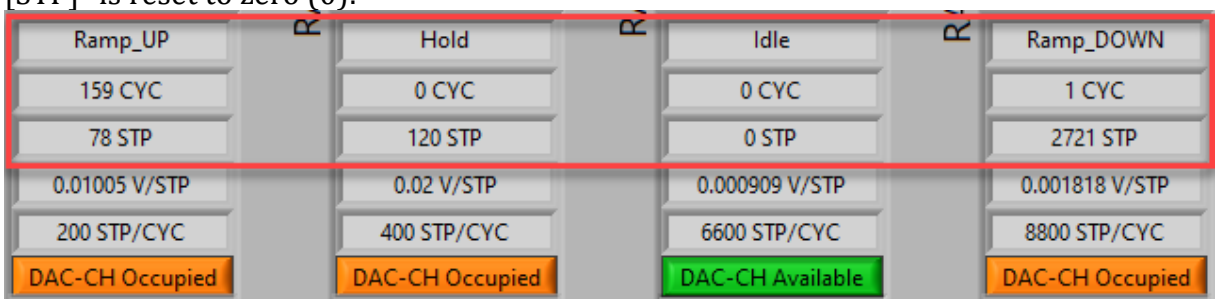
5.4 Start, Hold and Stop a RAMP/STEP-Generator

With the controls "Start A/B/C/D", "Hold A/B/C/D" and "Stop A/B/C/D" the corresponding RAMP-Generator can be controlled. In the "Hold" state the RAMP-Generator can be continued when pressing "Start" again or stopped by selecting "Stop". If all RAMP-Generators must be controlled in parallel the "Start ALL", "Hold ALL" and "Stop ALL" buttons can be used:



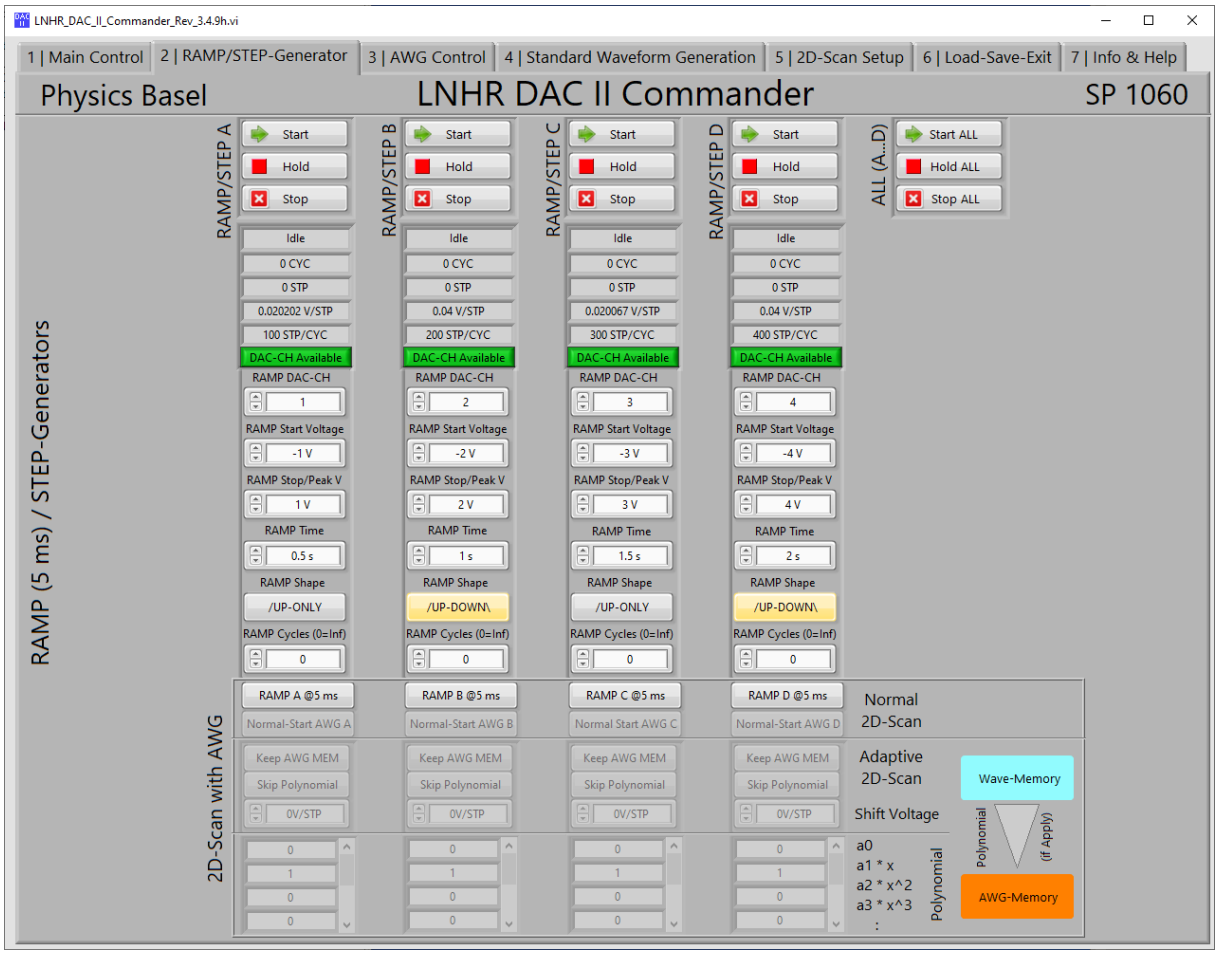
In the lower part the state of the RAMP-Generator is shown:
"Idle": The RAMP-Generator is inactive (stopped).
"Ramp_UP": The RAMP-Generator ramps UP.
"Ramp_DOWN": The RAMP-Generator ramps DOWN (in "/UP-DOWN\" mode only).
"Hold": The RAMP-Generator is in HOLD mode and its last voltage is on the DAC output.

Furter, the number of "CYCLEs-Done [CYC]" and the number of "STEPs-Done [STP]" is shown. When the RAMP-Generator is stopped ("Idle" state) the number of "STEPs-Done [STP]" is reset to zero (0):

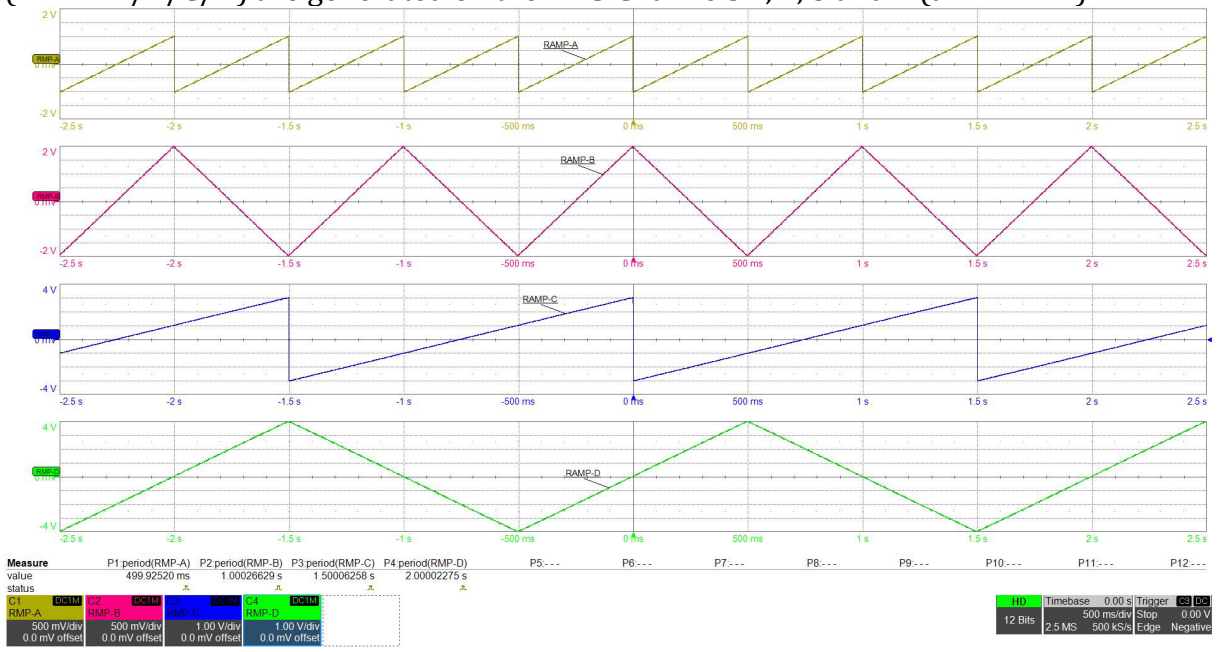


Note: If RAMP Shape is "/UP-DOWN\" the "STEPs-Done [STP]" counter first increments until the "RAMP Stop/Peak Voltage" is reached, then the counter decrements to zero where the "RAMP Start Voltage" is reached again.

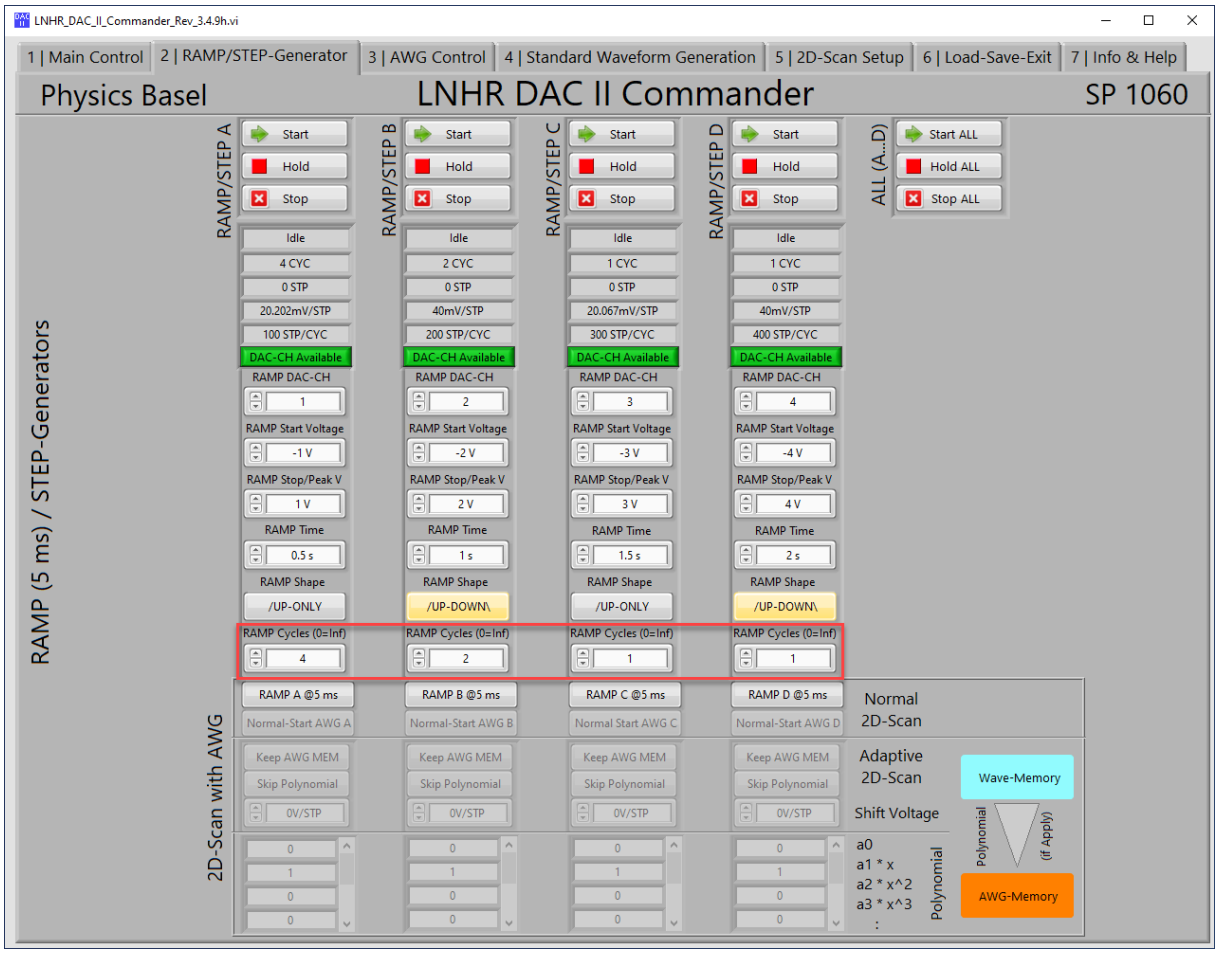
5.5 Examples: 4 x RAMP-Generators



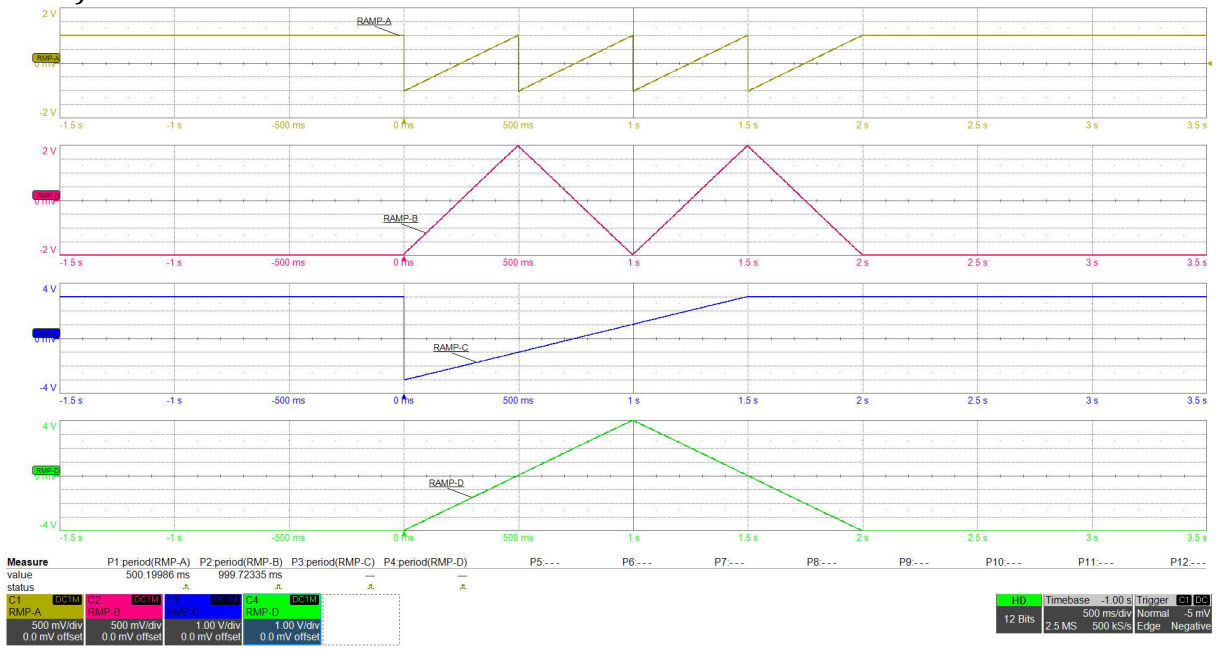
Example 1 has the above settings (all RAMPs run infinite) and the following RAMP-signals (RAMP-A/B/C/D) are generated on the DAC-Channels 1, 2, 3 and 4 (all in HWB):



The four RAMP-Generators are started synchronous by using the “Start ALL” button. Since the number of “RAMP Cycles (0=Inf)” is set to zero (0) the RAMPs run continuously. The measured periods, amplitudes and shapes corresponds to the set values.



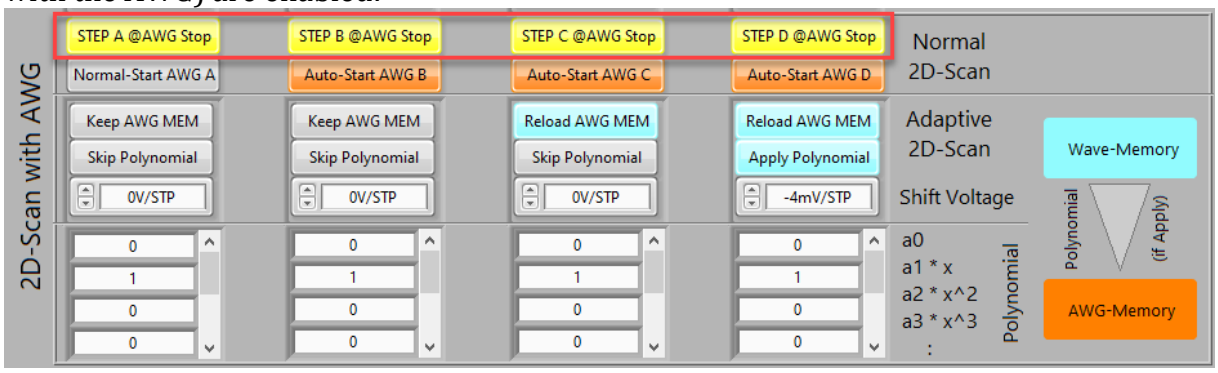
Example 2 has the above settings (RAMP Cycles: A=4, B=2, C=1, D=1) and the following RAMP-signals (RAMP-A/B/C/D) are generated on the DAC-Channels 1, 2, 3 and 4 (all in HWB):



The four RAMP-Generators are started synchronous by using the “Start ALL” button. The number of “RAMP Cycles (0=Inf)” is restricted to four (4) for RAMP-A, to two (2) for RAMP-B and to one (1) for RAMP-C and RAMP-D.

5.6 Select STEP Mode

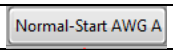
If a STEP function should be performed, the corresponding button "STEP A/B/C/D @AWG Stop" must be selected; then the parameters for the STEP-Generator (needed for 2D-Scan with the AWG) are enabled:



In STEP Mode the RAMP/STEP-Generator is no longer running with a fixed update period of 5 msec. It is triggered when the corresponding AWG is stopped. The next voltage STEP is applied when the AWG has finished. The typical time-delay from AWG finished to the next STEP voltage is around 7.5 msec and varies between 5 and 10 msec depending on the actual AWG Duration/Period [sec].
A single-cycle ramp-function programmed on the AWG results in a 2D-Scan. The fast output of the AWG (ramp-function) is the y-axis while the output of the STEP-Generator is the x-axis. For user friendly building 2D-Scans see chapter "Tab 5 | 2D-Scan Setup".

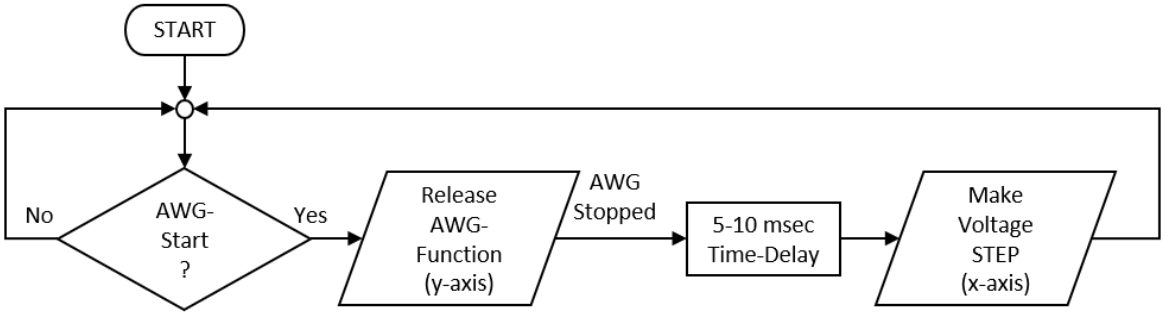
The following settings for the STEP-Generator / 2D-Scan can be made:

5.6.1 Normal-Start AWG



"Normal-Start AWG" means that the AWG will start normally by either an external TTL signal on the back panel (Trig In AWG) or by a remote command or by pressing the button "Start AWG" on "Tab 3 | AWG Control"; this is called an AWG Start event.

Each individual y-line of a 2D-Scan must be initiated by such an AWG Start event. After the first y-line is finished (AWG Stopped), the STEP-Generator makes its first STEP and then switches to the "Hold" state. Now the number of "STEPs-Done [STP]" is increased from zero (0) to one (1). The STEP-Generator waits in the "Hold" state until the next y-line has finished (AWG Stopped) and the number of "STEPs-Done [STP]" is incremented. In order to go through a full 2D scan, the AWG must be restarted repeatedly until the STEP-Generator reaches the "Idle" state. The flowchart below shows the behavior of a 2D-Scan in the "Normal-Start AWG" mode with "Keep AWG MEM" selected:



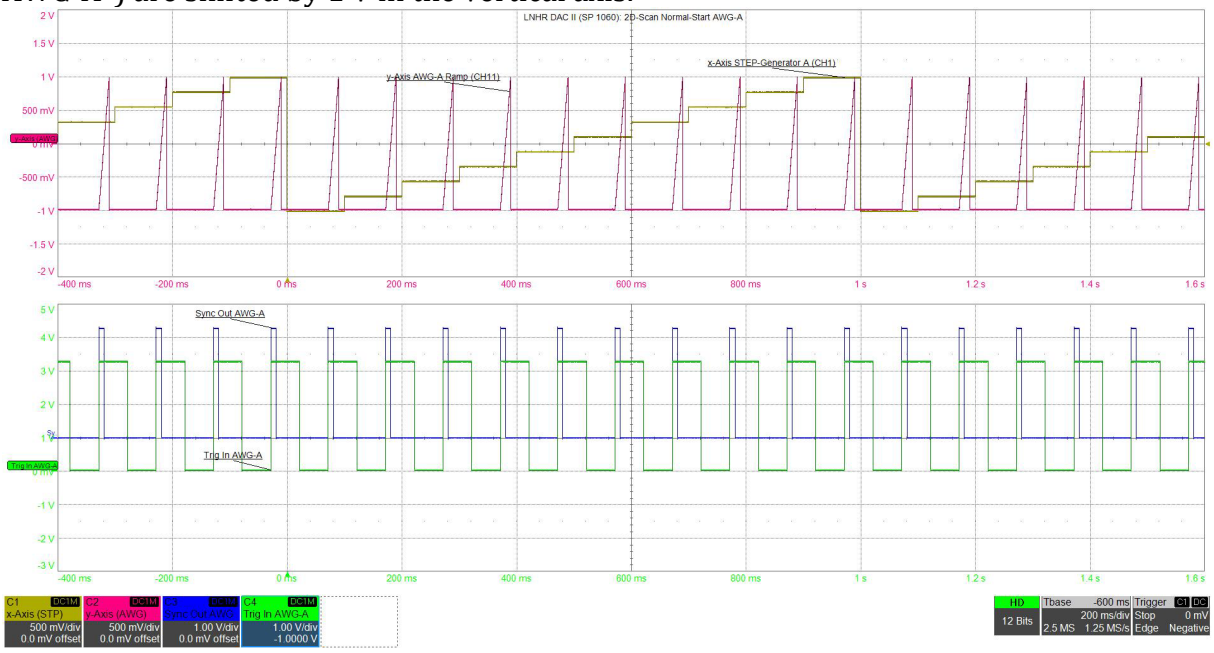
Note: If the STEP-Generator is in the "Idle" state and an AWG Start event is detected, the 2D-Scan is automatically restarted. Therefore, the control software must detect the "Idle" state of the STEP-Generator and then stop the AWG Start event to end a 2D-Scan properly.

The time-delay between two y-lines, triggered by an AWG Start, is under the user's full control. This can be useful when the DAQ takes a long time to store/process the measured data of a single y-line. In this case the 2D-Scan implemented on the LNHR DAC II is timed by the DAQ – the DAQ is the timing master while the LNHR DAC II is the timing slave.

The time-delay from AWG Stopped to the update of the STEP-Generator is around 7.5 msec; it can vary between 5 msec and 10 msec depending on the duration/period of the programmed AWG function.

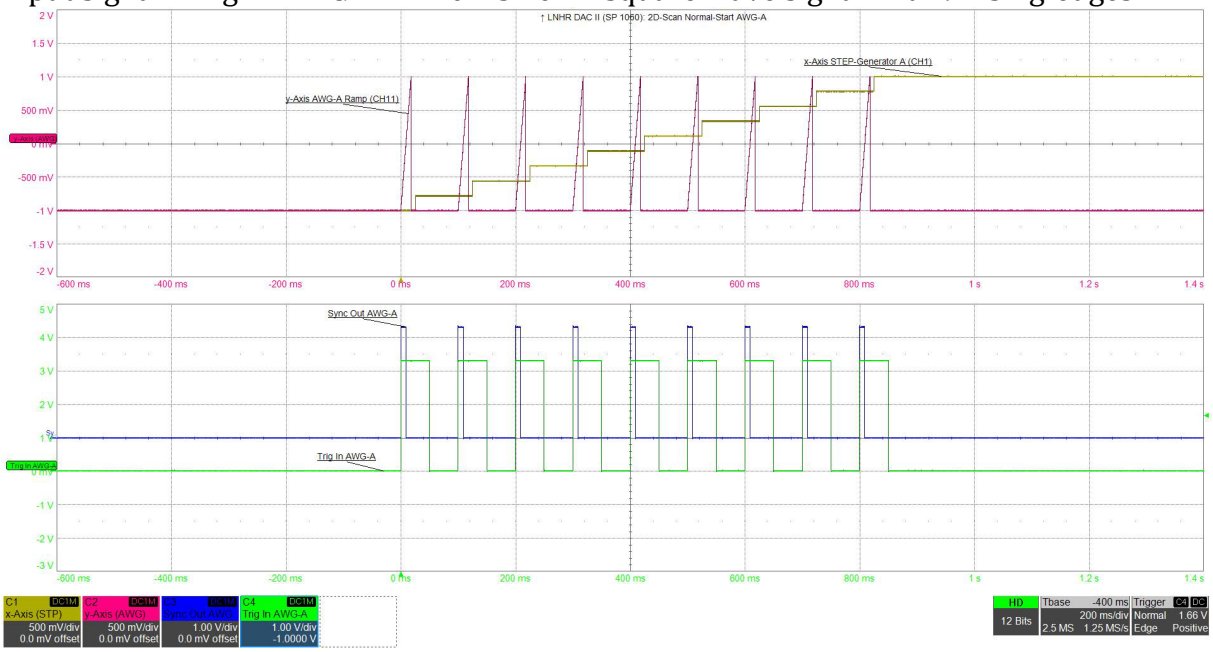
Note: The minimum time-delay between two y-lines (two AWG Start) is given by the "AWG Duration/Period [sec]" plus 15 msec; when the AWG-Memory is kept ("Keep AWG MEM").

Below an infinite-run 2D-Scan in "Normal-Start AWG" mode with 10 "x-axis voltage-levels" within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1'000 points) is shown.
The AWG-A is started on the rising-edge of the external TTL-input signal "Trig In AWG-A" which is connected to a 10 Hz square wave source (100 msec period). The upper grid shows the x- and y-axis voltages (x-axis = yellow, y-axis = red). On the lower grid the synchronization output signal ("Sync Out AWG-A" = blue) and the AWG trigger input signal ("Trig In AWG-A" = green), coming from an external function generator, is displayed. For reasons of clarity the two digital signals ("Sync Out AWG-A" and "Trig In AWG-A") are shifted by 1 V in the vertical axis.



Every 100 msec (10 Hz) the AWG-A gets externally triggered and the "Sync Out AWG-A" output signal (which indicates the start of the AWG) is generated; this synchronization signal is high for the first half of the AWG-points which in this example last 9 msec. After the single-cycle AWG-A has stopped, the STEP-Generator A is updated and then waiting in the "Hold" state for a next AWG Start event.

A single-run 2D-Scan in "Normal-Start AWG" mode with 10 "x-axis voltage-levels" within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1'000 points) is shown below. The AWG-A is started on the rising-edge of the external TTL-input signal "Trig In AWG-A" which is 10 Hz square wave signal with 9 rising-edges:



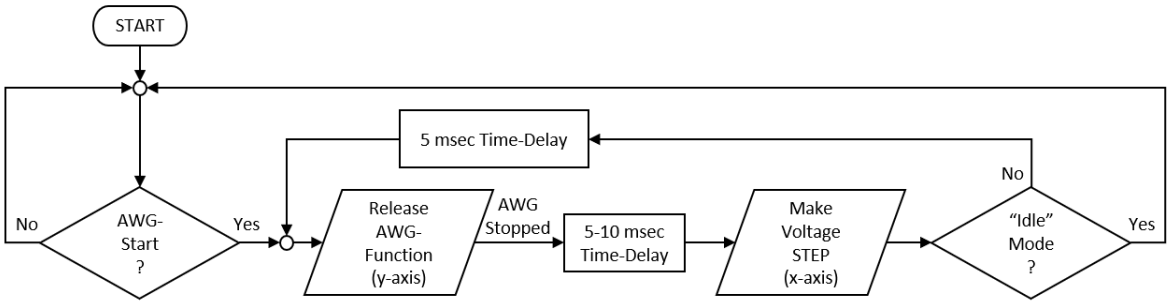
Note: After 9 y-lines the STEP-Generator reaches the "Idle" state, since the x-Step to + 1 V is the last of the 10 "x-axis voltage-levels". Therefore, in the "Normal-Start AWG" mode the "Idle" state is reached after "x-axis voltage-levels" – 1 (minus one) AWG Start events have arrived.

5.6.2 Auto-Start AWG

Auto-Start AWG A

If "Auto-Start AWG" is selected, the AWG gets automatically restarted after the STEP-Generator is updated. A fixed time-delay of 5 msec is implemented from the update of the STEP-Generator to the restart of the AWG. This time-delay of 5 msec is only valid when the AWG-Memory is kept and not reloaded; therefore, "Keep AWG MEM" must be selected. In case the AWG-Memory has to be reloaded before its start ("Reload AWG MEM" selected) this time-delay is longer and is depending on the size of the AWG-Memory; for details see the chapters "Keep AWG MEM" and "Reload AWG MEM".

A 2D-Scan can be initiated by a single external TTL signal on the back panel (Trig In AWG) or by a remote command or by pressing the button "Start AWG" on "Tab 3 | AWG Control"; this is called an AWG Start event. After the first AWG Start event is detected, a complete 2D-Scan runs automatically at maximum speed. The flowchart below shows the behavior of a 2D-Scan in the "Auto-Start AWG" mode with "Keep AWG MEM" selected:

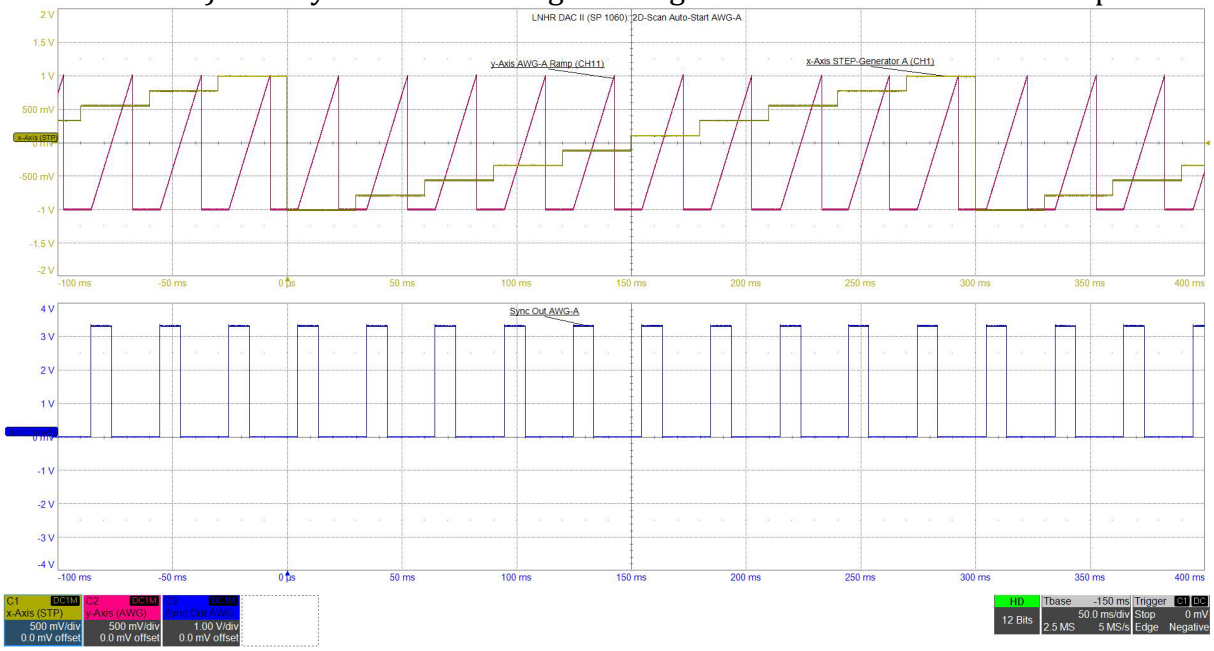


The time-delay from AWG Stopped to the update of the STEP-Generator is around 7.5 msec; it can vary between 5 msec and 10 msec depending on the duration/period of the programmed AWG function.

Note: For a reliable auto-start, the "AWG Duration/Period [sec]" must be at least 6 msec. Avoid overloading the device by sending a large number of remote commands while running 2D-Scans in Auto-Start mode. Otherwise, the 2-Scan can be interrupted.

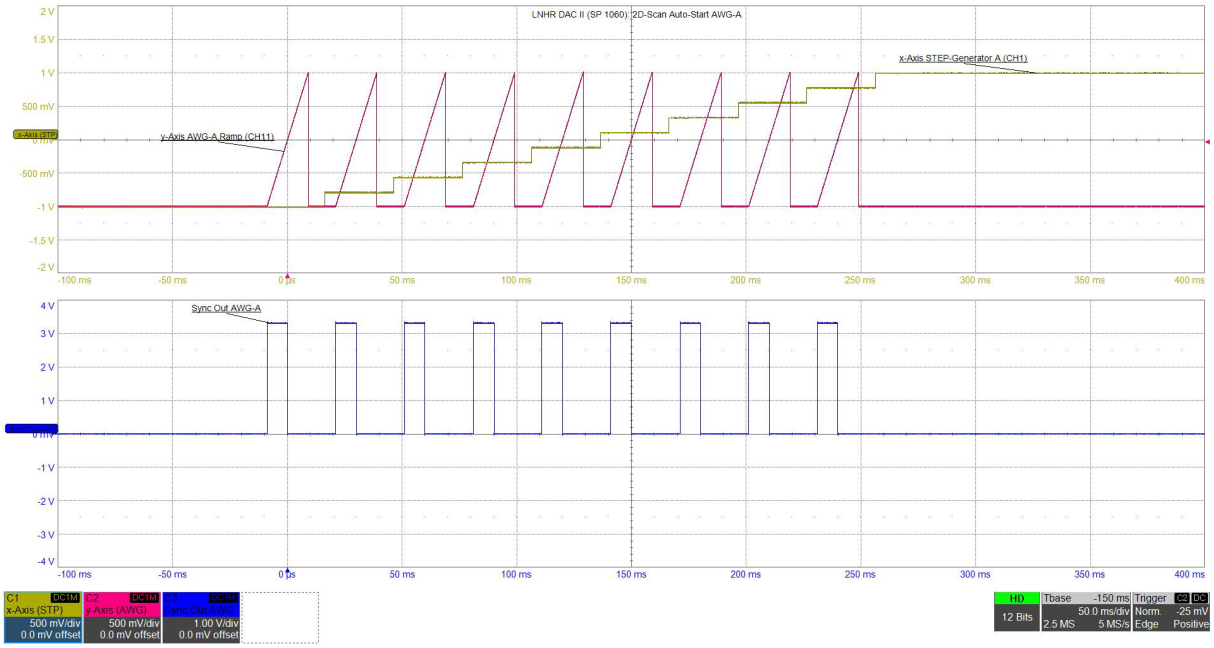
The y-axis synchronization of the DAQ can be done by using the AWG synchronization output "Sync Out AWG" on the back panel. In this case the 2D-Scan implemented on the LNHR DAC II makes the timing for the DAQ – the LNHR DAC II is the timing master while the DAQ is the timing slave.

Below an infinite running 2D-Scan in "Auto-Start AWG" mode with 10 "x-axis voltage-levels" within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1'000 points) is generated. The upper grid shows the x- and y-axis voltages (x-axis = yellow, y-axis = red) and on the lower grid the synchronization output signal ("Sync Out AWG-A" = blue). This synchronization signal is high for the first half of the AWG-points:



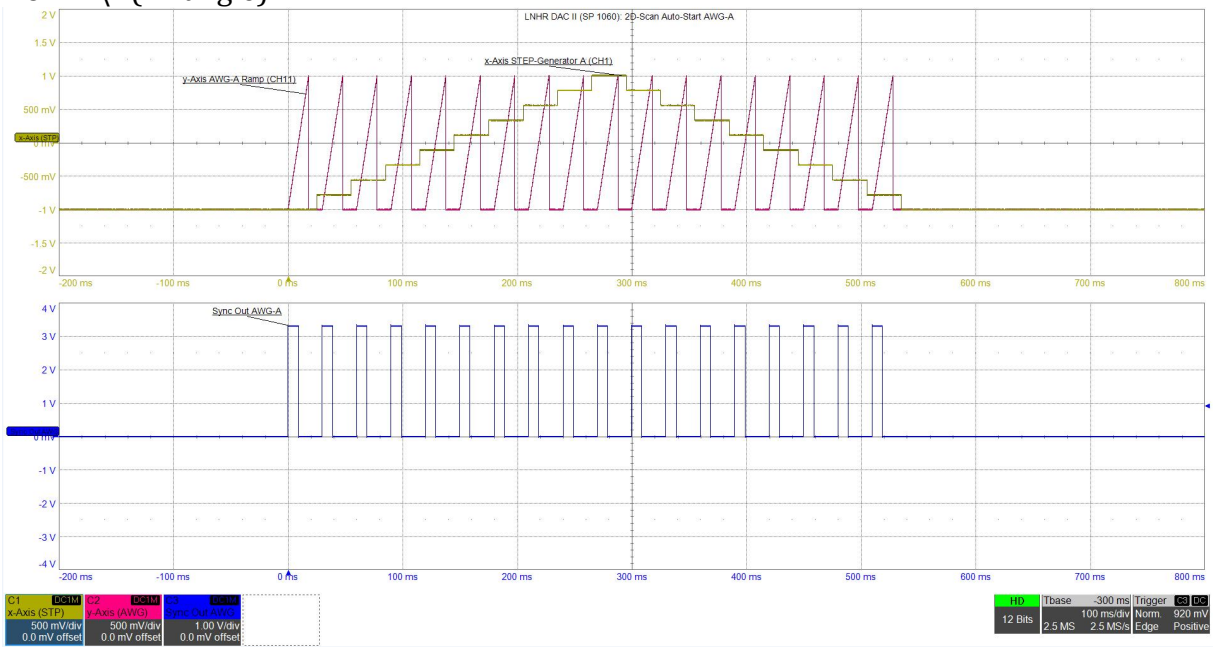
In this mode the maximum speed of a 2D-Scan is reached and the DAQ must be synchronized by the output signal "Sync Out AWG".

A single-run 2D-Scan in "Auto-Start AWG" mode with 10 "x-axis voltage-levels" within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1'000 points) is shown below:



Note: Only 9 y-lines are generated since the last x-Step to + 1 V ends the 2D-Scan and the AWG isn't automatically restarted again – otherwise the 2D-Scan would start over. Therefore, in the "Auto-Start AWG" mode "x-axis voltage-levels" – 1 (minus one) y-lines are generated when Ramp Shape is "/UP-ONLY" (Sawtooth).

The same single-run 2D-Scan as above is shown below, but the Ramp Shape is set to "/UP-DOWN\" (Triangle):



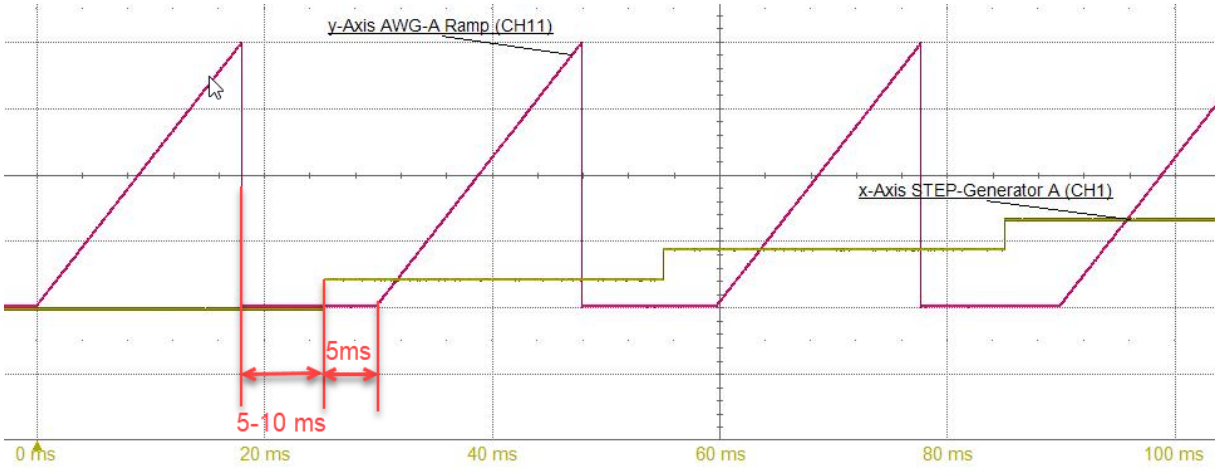
Note: Only 18 y-lines are generated since the last x-Step to 0 V ends this 2D-Scan and the AWG isn't automatically restarted again – otherwise the 2D-Scan would start over. Therefore, in the "Auto-Start AWG" mode (2 * "x-axis voltage-levels") – 2 (minus two) y-lines are generated when Ramp Shape is "/UP-DOWN\" (Triangle).

5.6.3 Keep AWG MEM

Keep AWG MEM

When "Keep AWG MEM" is selected, all y-axis lines of a 2D-Scan are identical. The same predefined AWG function is recalled for each y-axis. This means that no adaption is made in the y-axis during a running 2D-Scan. Such a 2D-Scan is faster since the AWG-Memory hasn't to be reloaded before a next y-axis can be started.

If "Auto-Start AWG" is selected, a fixed time-delay of 5 msec is implemented from the update of the STEP-Generator to the automatic restart of the AWG. In this case, a 2D-Scan runs automatically at maximum speed. The detailed timing in the "Auto-Start AWG" mode is given below:



The time-delay from AWG Stopped to the update of the STEP-Generator is around 7.5 msec; it can vary between 5 msec and 10 msec depending on the duration/period of the programmed AWG function.

5.6.4 Reload AWG MEM

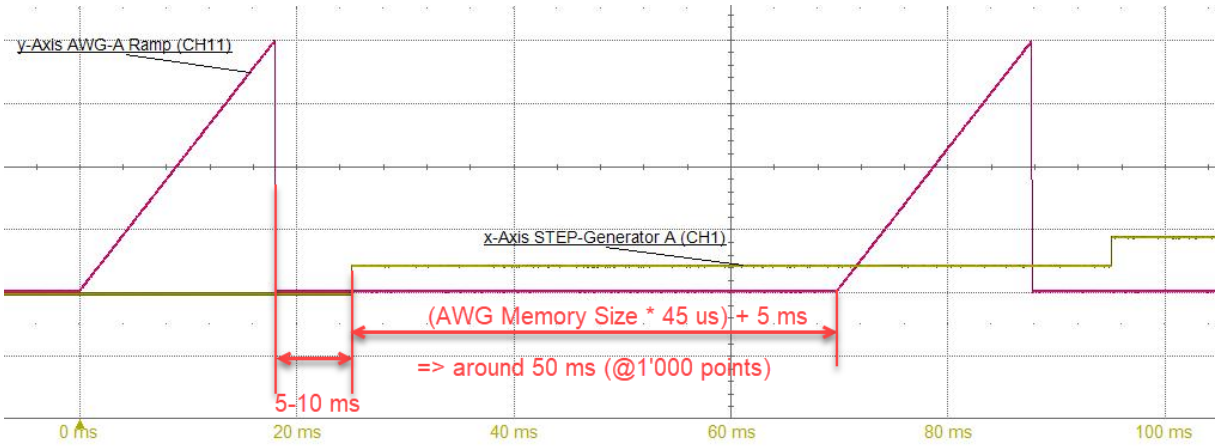
Reload AWG MEM

When "Reload AWG MEM" is selected, the AWG-Memory is reloaded after each y-axis line is finished. Reload means that the WAVE-Memory (reference) is copied to the AWG-Memory where the shape of the y-axis is stored. This allows to modify the y-axis function during a running 2D-Scan; this is called an "Adaptive 2D-Scan". With such an "Adaptive 2D-Scan" the y-axis function can be adapted depending on the x-axis.

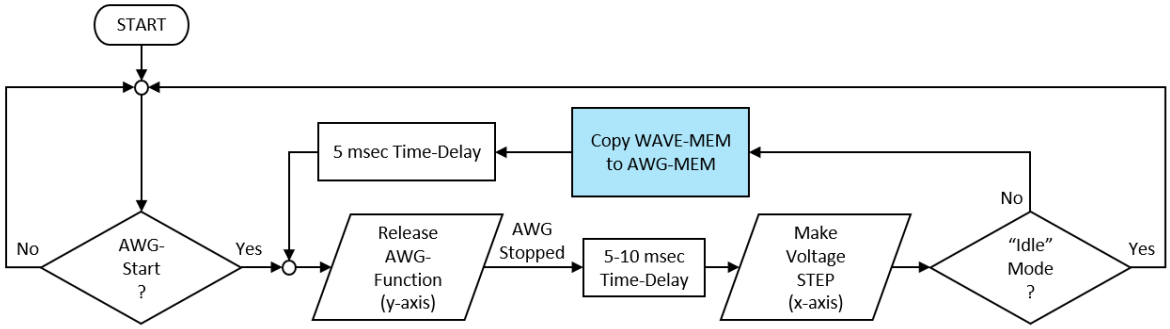
If "Auto-Start AWG" is selected, the time-delay from the update of the STEP-Generator to the automatic restart of the AWG is depending on the size of the AWG-Memory. Each AWG point needs around 45 µsec to be copied from the WAVE-Memory to the AWG-Memory. The exact time per point is depending on the CPU-Load; the total time-delay (Total TD) can be estimated by "AWG Memory Size" times 45 µsec plus the fixed time-delay of 5 msec:

$$Total\ TD = (AWG\ Memory\ Size \cdot 45\ \mu sec) + 5\ msec$$

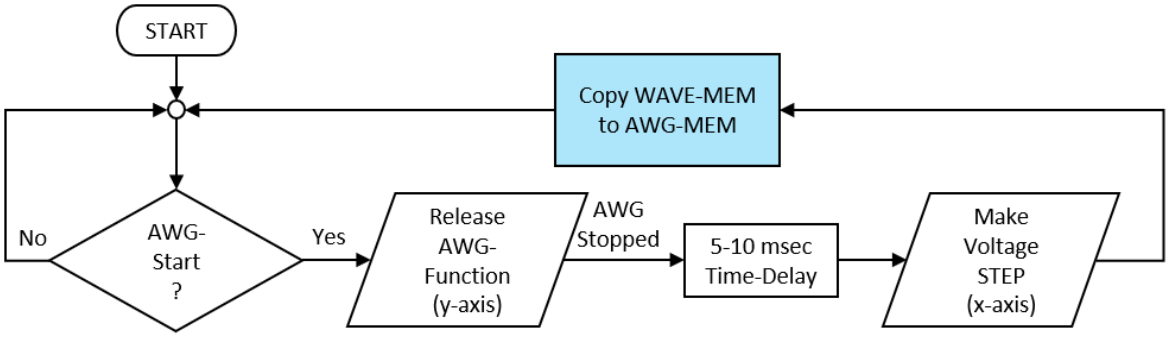
For an "AWG Memory Size" of 1'000 points this total time-delay is around 50 msec which is a factor of ten longer than in the "Keep AWG MEM" mode. The detailed timing in the "Auto-Start AWG" mode with an "AWG Memory Size" of 1'000 points is given below:



Below the flowchart with selected "Reload AWG MEM" in the "Auto-Start AWG" mode is shown:



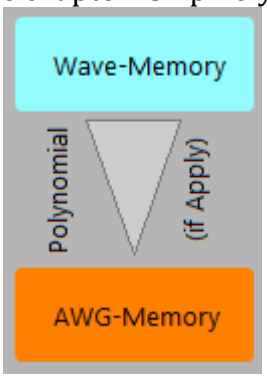
Below the flowchart with selected "Reload AWG MEM" in the "Normal-Start AWG" mode is given:



Note: If "Normal-Start AWG" is selected, the minimum time-delay between two y-lines (two AWG Start) is given by the "AWG Duration/Period [sec]" plus the total time-delay (Total TD) plus 10 msec. In the example above this would result in a minimum retrigger time of 78 msec (18 msec + 50 msec + 10 msec), corresponding to maximum y-axis retrigger frequency of 12. 8 Hz.

In principle, the WAVE-Memory can be updated during a running 2D-Scan, but writing the complete WAVE-Memory from the host computer is quite time-consuming. For each y-scan line a completely new WAVE-Memory would have to be written before the AWG memory can be copied and a next y-scan line can be started.

A much more time efficient method is to keep the same WAVE-Memory as a reference and only adapt the Polynomial which is applied when the AWG-Memory is written. Since the new polynomial coefficients can be written to the LNHR DAC II in a very short time, the control software can adapt the y-axis on its own algorithm. For this option the "Apply Polynomial" has to be selected – see chapter "Skip Polynomial" and "Apply Polynomial":

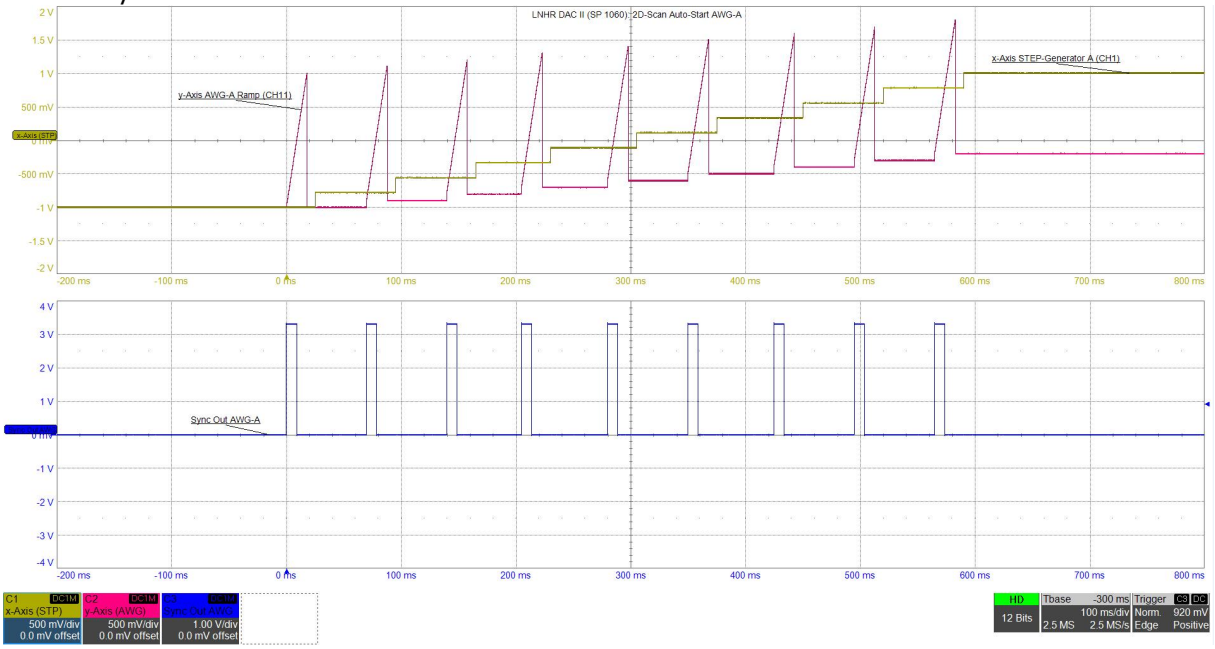


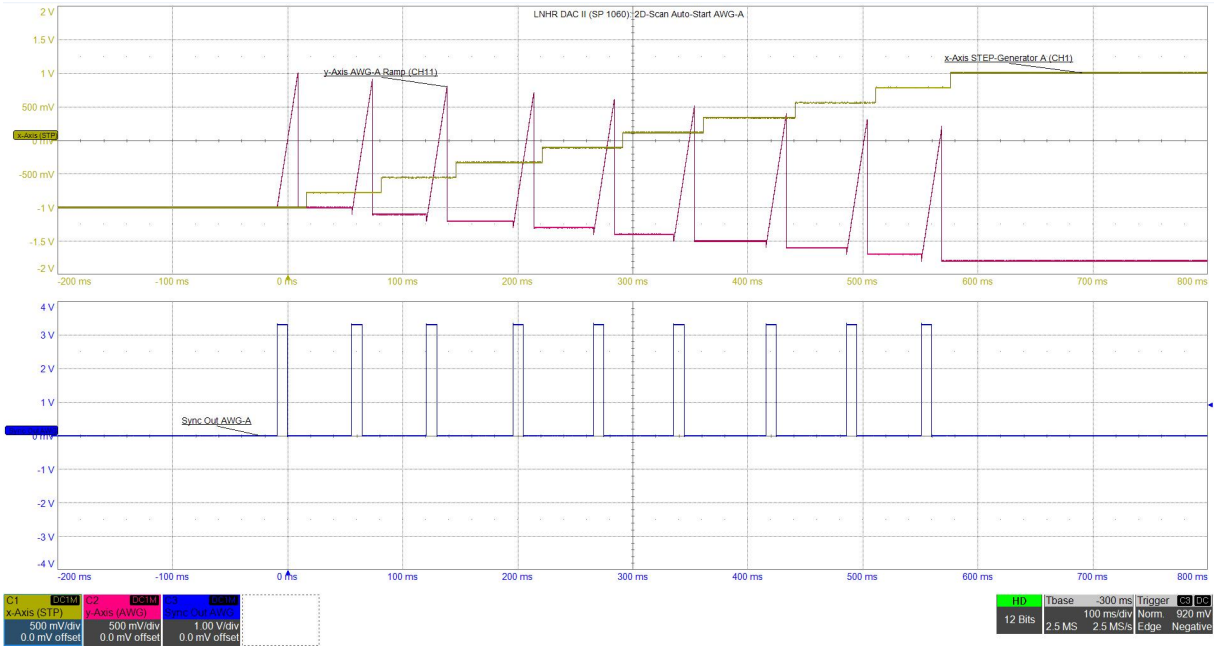
If only a linear offset adaption of the y-axis versus the x-axis is to take place, the parameter "Shift Voltage [V/STP]" can be used. After each x-axis step the polynomial coefficient a0 (offset) gets automatically modified to the new value which is given by:

$$a0\ [V] = STEPs\ Done\ [STP]\ \cdot Shift\ Voltage\ [\frac{V}{STP}]$$

This leads to a linear offset voltage of the y-axis depending on the x-axis; a rhombus shaped 2D-Scan is generated. Assuming a set "Shift Voltage [V/STP]" of -1 mV/STP and the "STEPs-Done [STP]" is at 566, the y-axis will have an offset voltage of -566 mV. Since the polynomial coefficient a0 (offset) is modified during the running 2D-Scan, the "Apply Polynomial" has to be selected. If a "Shift Voltage [V/STP]" of 0 (zero) mV/STP is set the polynomial coefficient a0 isn't modified. See also the chapters "Shift Voltage" and "Polynomial Coefficients".

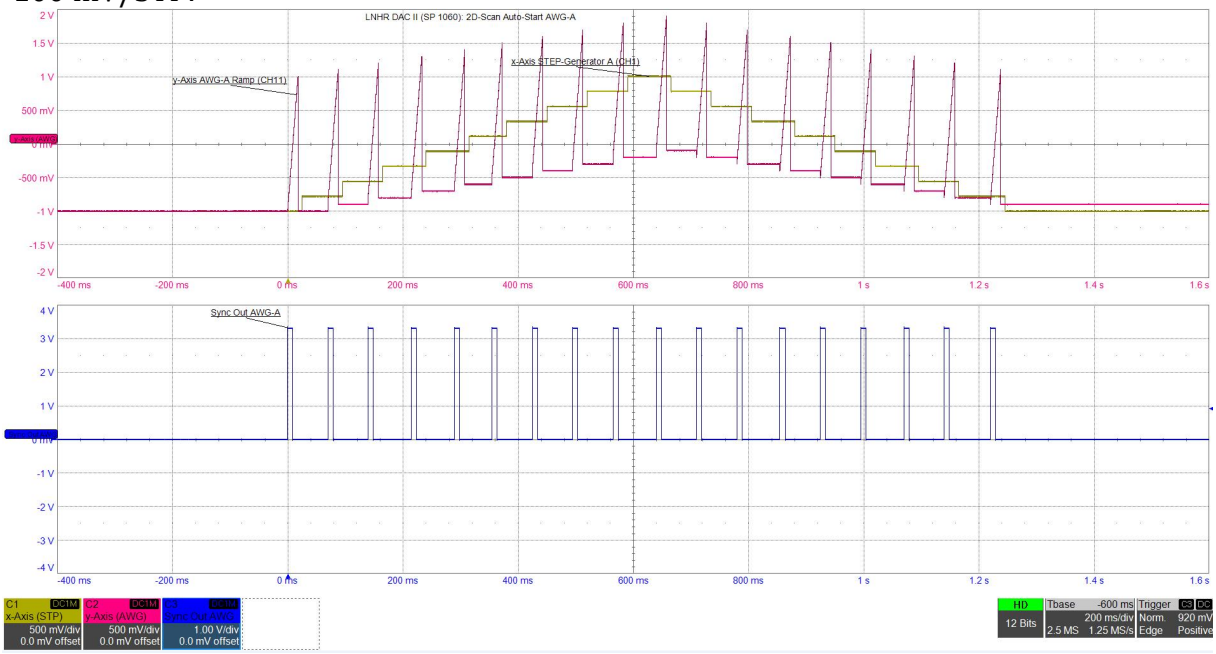
The two examples below show a single-run adaptive 2D-Scan in "Auto-Start AWG" mode with 10 "x-axis voltage-levels" within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1'000 points). The Ramp Shape is set to "/UP-ONLY" (Sawtooth). In the first plot a "Shift Voltage [V/STP]" of +100 mV/STP is set and in the second plot -100 mV/STP:

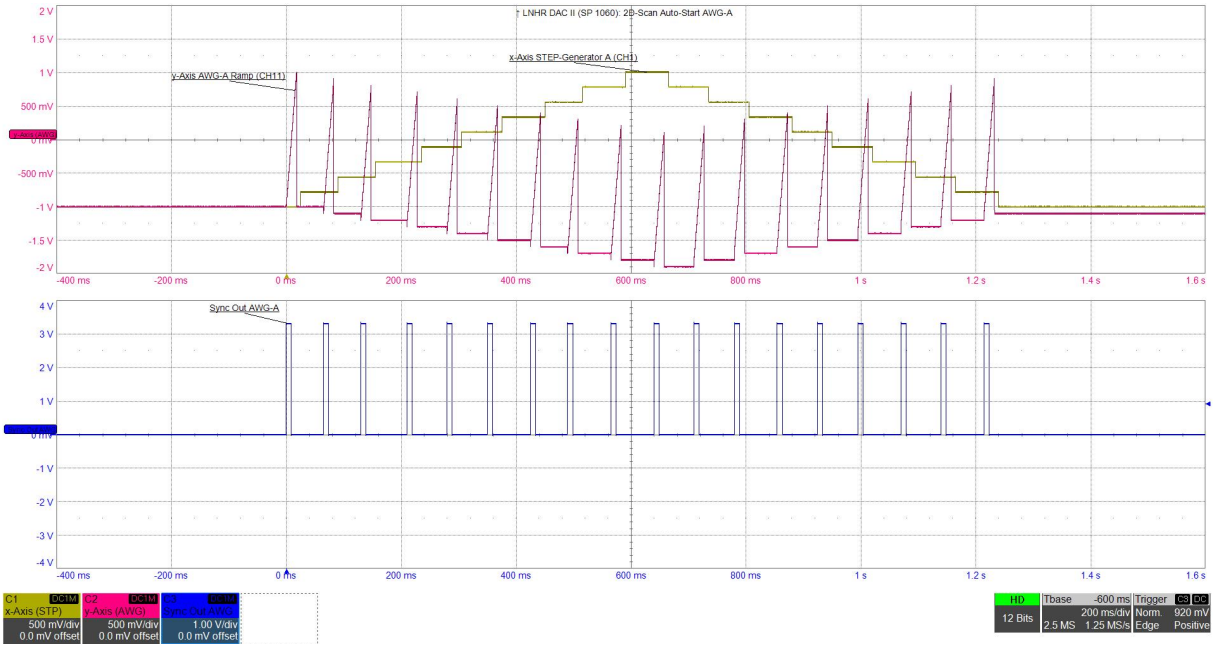




After each step the y-axis is shifted by +100 mV (top) respective -100 mV (bottom). At the last y-line the "STEPs-Done [STP]" is incremented to 8 and therefore the y-axis shift voltage reaches +800 mV (top) respective -800 mV (bottom).

The two examples below show a single-run adaptive 2D-Scan in “Auto-Start AWG” mode with 10 “x-axis voltage-levels” within a ±1 V range and an AWG ramp-function (±1 V) with a duration of 18 msec (1’000 points). The Ramp Shape is set to “/UP-DOWN\” (Triangle). In the first plot a “Shift Voltage [V/STP]” of +100 mV/STP is set and in the second plot -100 mV/STP:





Since the “STEPs-Done [STP]” counter is incremented to 9 (where the x Peak Voltage is reached) before it is decremented to zero, also the y-axis is first up and then down. The shift per x-axis step is +100 mV (top) respective -100 mV (bottom). At the x Peak Voltage where the “STEPs-Done [STP]” are 9 also the peak y-axis shift voltage of +900 mV (top) respective -900 mV (bottom) is reached.

5.6.5 Skip Polynomial

Skip Polynomial

When "Skip Polynomial" is selected, the WAVE-Memory (reference) is copied to the AWG-Memory without applying the Polynomial; it is ignored.
If the shape of the y-axis shall be modified during a running 2D-Scan (adaptive 2D-Scan), the only way is to update the complete WAVE-Memory from the host computer, which is quite time-consuming.

5.6.6 Apply Polynomial

Apply Polynomial

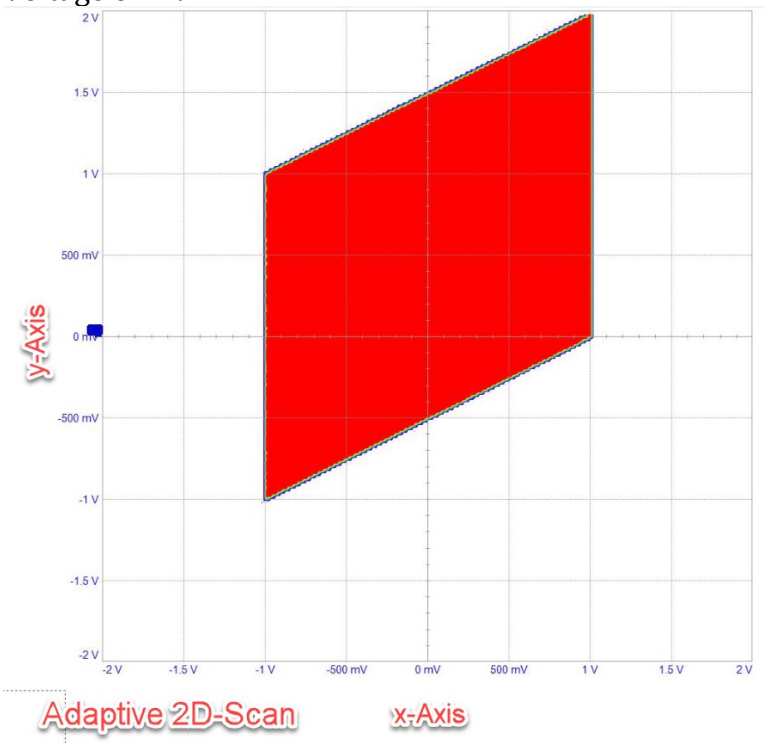
When "Apply Polynomial" is selected, the WAVE-Memory (reference) is copied to the AWG-Memory by applying the given actual Polynomial.
Applying such a Polynomial is a highly efficient method for generating adaptive 2D-Scans. Only a few new polynomial coefficients have to be written from the host computer to LNHR DAC II to adapt the shape of the y-axis.
With the default polynomial coefficients (all zero, except a1=1), the AWG-Memory corresponds exactly to the WAVE-Memory (reference). If the polynomial coefficient a0 (offset) is set to 0.2 (for example) while the coefficient a1 (linear coefficient) is still at one (1), the y-axis Voltage gets shifted by 0.2 V.

5.6.7 Shift Voltage [V/STP]

0V/STP

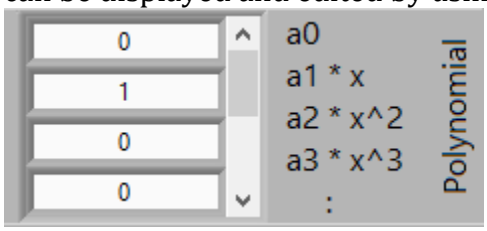
The parameter "Shift Voltage [V/STP]" can be used for a linear offset adaption of the y-axis versus the x-axis.
After each x-axis step the polynomial coefficient a0 (offset) gets automatically modified to the new value which is given by the "Shift Voltage [V/STP]" multiplied by the "STEPs-Done [STP]"; this leads to a linear adaptive 2D-Scan (rhombus shaped). See also chapter "Reload AWG Memory".

Below you can see the xy-plot a linear adaptive 2D-Scan with a resolution of 1'000 * 1'000 xy-points and a voltage span of ±1 V in both axes; the "Shift Voltage [V/STP]" is set to 1 mV/x-Step: This 1 mV/x-Step multiplied by the 1'000 x-points result in a total y-Shift-Voltage of 1 V:



5.6.8 Polynomial Coefficients

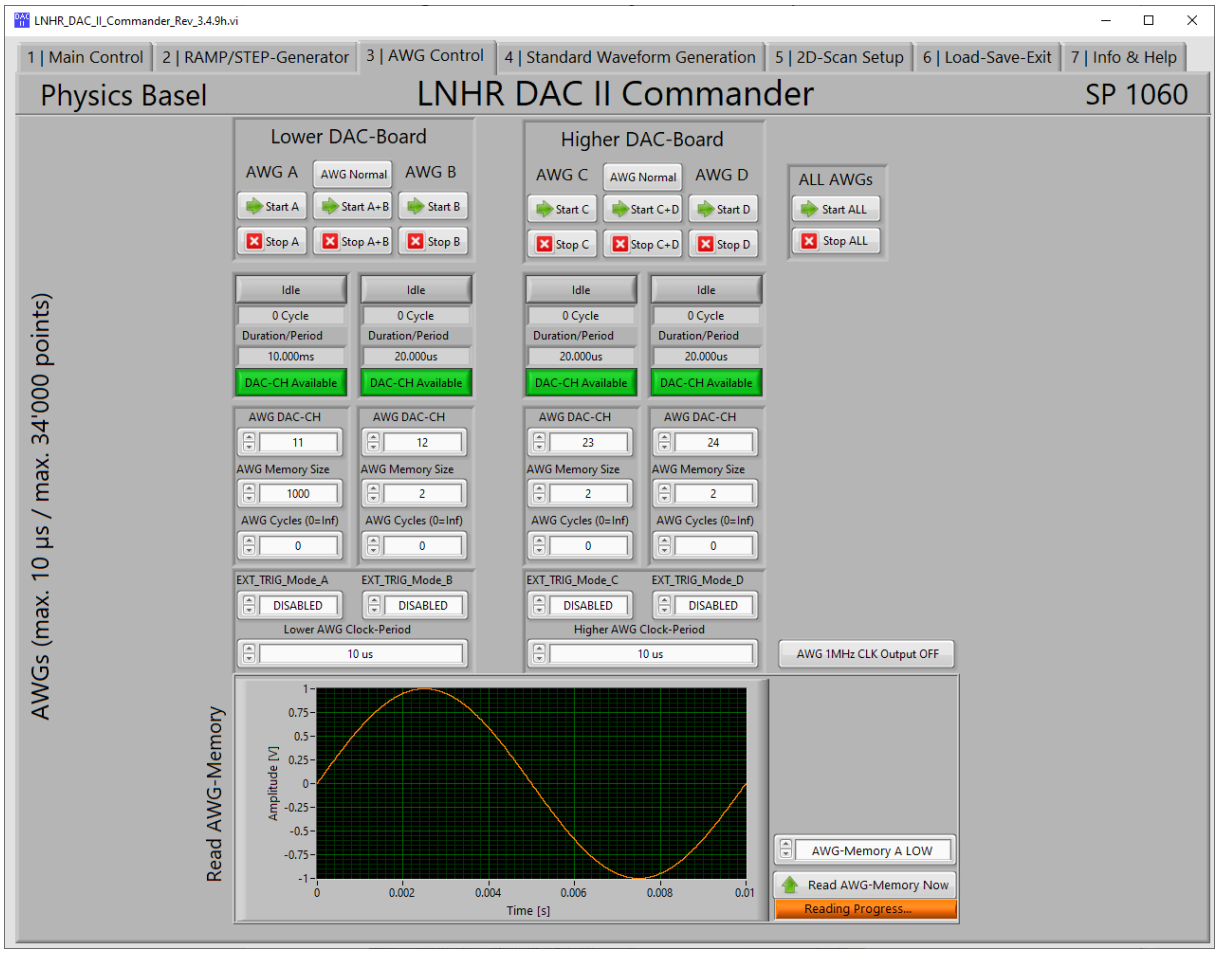
During copying the WAVE-Memory (reference) to the AWG-Memory this Polynomial gets applied, if “Apply Polynomial” is selected. The Polynomial Coefficients are in ascending order and a0 (offset) to a3 (x^3) are shown. Also, higher-order Polynomial Coefficients can be displayed and edited by using the scroll-bar on the right:



The default polynomial coefficients are all zero (0), except a1 (linear coefficient) which is set to one (1). This results in a one-to-one copy of the WAVE-Memory (reference) to the AWG-Memory even when “Apply Polynomial” is selected.

When the polynomial coefficients a1 (linear coefficient) is set to two (2), for example, the content of WAVE-Memory (reference) gets multiplied by a factor two (2) while writing to the AWG-Memory. In a 2D-Scan this results in a y-axis which is stretched by a factor of two (2).
The polynomial coefficient a0 (offset) can be used for an adaptive 2D-Scan. Since this polynomial coefficient a0 can be updated by the host computer after each y-axis scan, also nonlinear adaptive 2D-Scans can be implemented.

6 Tab 3 | AWG Control



The parameters and the modes of the four individual AWGs (A, B, C, D) can be set on this Tab. Further the AWGs can be start and stop here.
In the example above, a sine function with a frequency of 100 Hz and an amplitude of 1 V_{peak} has been generated and written to the AWG-Memory A by using the "Tab 4 | Standard Waveform Generation" – see chapter "Standard Waveform Generation".

6.1 Start and Stop AWGs

With the controls "Start A/B/C/D" and "Stop A/B/C/D" the correspondin g AWGs can be controlled. If all AWGs must be controlled in parallel the "Start ALL" and "Stop ALL" buttons can be used. In addition, the two AWGs on one DAC-Board can be controlled synchronously by using the buttons "Start A+B" and "Stop A+B" (Lower DAC-Board) respective "Start C+D" and "Stop C+D" (Higher DAC-Board):

6.1.1 AWG Normal / AWG Only

The AWG time-jitter can be reduced by switching to the "AWG Only" mode where the DAC-Board is exclusively working for the AWG function. This option can be set individually for each of the two DAC-Boards: Lower DAC-Board = "AWG A/B Only", Higher DAC-Board = "AWG C/D Only". If "AWG Only" is selected, all other DAC-Channels of the corresponding DAC-Board will be blocked and its last DAC voltages will be frozen and can no longer be updated.

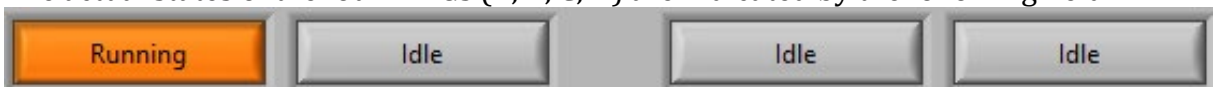
In the "AWG Normal" mode the AWG works in a mixed mode together with the normal DAC output including the RAMP/STEP-Generators – the drawback is that the time-jitter of the AWG function is slightly higher.

6.2 AWG Settings / Information

The field below shows the Settings and Information related to the four AWGs (A, B, C, D):

6.2.1 States of the AWGs

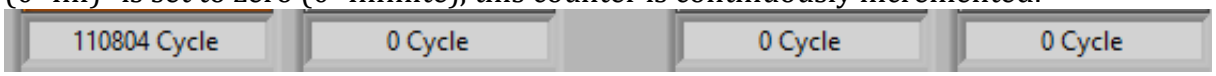
The actual states of the four AWGs (A, B, C, D) are indicated by the following field:



If the AWG is started the indicator "Running" is shown; a stopped AWG shows "Idle".

6.2.2 Number of AWG Cycles Done

The "Number of AWG Cycles Done" shows the AWG cycles finished – if the "AWG Cycles (0=Inf)" is set to zero (0=Infinite), this counter is continuously incremented:



If the AWG has not yet started, the corresponding "Number of AWG Cycles Done" is set to zero (0).

6.2.3 AWG Duration/Period Information

The "Duration/Period" is the length of a complete single AWG Cycle; it is calculated from the "AWG Memory Size" multiplied by the "AWG Clock-Period". In our example the "AWG-A Memory Size" is 1'000 and the "Lower AWG Clock-Period" is 10 µsec resulting in a "Duration/Period" of 10 msec (1'000 * 10 µsec = 10 msec):

The default "AWG Memory Size" is two (2) and the default "AWG Clock-Period" is 10 µsec, therefore the default "Duration/Period" is 20 µsec.

6.2.4 Select AWG DAC-Channels

The user can define the DAC-Channel on which to output the AWG function. The DAC-Chanel range is restricted to 1…12 for AWG-A/B (Lower DAC-Board) and to 13…24 for AWG-C/D (Higher DAC-Board). If the selected "AWG DAC-CH" is available (not used by another RAMP or AWG) the indicator "DAC-CH Available" is green:

If a DAC-Channel is double-used, the warning "DAC-CH Occupied" is generated:

Note: On a running AWG the flag "DAC-CH Occupied" is displayed and all the AWG Parameters are disabled and greyed out.

6.2.5 Set AWG Memory Size

The "AWG Memory Size" can be in a range from 2…34'000; the default "AWG Memory Size" is two (2).

Note: When a waveform is generated by using the "Tab 4 | Standard Waveform Generation" and then written to the AWG-Memory, the corresponding "AWG Memory Size" gets automatically updated to cover a complete AWG cycle. See also chapter "Standard Waveform Generation".

6.2.6 Set AWG Cycles

The number of AWG Cycles can be set by the parameter "AWG Cycles (0=Inf)" which must be in a range from 0 to 4E9 Cycles. If it is set to zero (0) the AWG runs infinitely and then it must be stopped by the user:

In the example above the AWG-A runs infinitely, the AWG-B makes 111 Cycles, the AWG-C one (1) Cycle and the AWG-D 2'222 Cycles.

6.2.7 Select External AWG Trigger Mode

The four AWGs (A, B, C, D) can be triggered (started/stopped/stepped) by an external TTL signal applied to the "Trig In AWG-A, B, C, D" input on the back panel. The behavior of these external AWG Trigger input signals can be selected as "DISABLED", "START only", "START-STOP" or "SINGLE-STEP". The default mode is "DISABLED":

In the "DISABLED" mode, the external AWG Trigger input signal is ignored. In the "START only" mode, the AWG is started on the rising-edge of the AWG Trigger input. In the "START-STOP" mode, the AWG is started on the rising-edge and stopped on the falling-edge of the external AWG Trigger input signal. In this mode the AWG runs as long as the external AWG Trigger input is high.
In the "SINGLE-STEP" mode, the AWG gets clocked on the rising edge of the external input; the frequency ranges from DC up to 100 kHz and the minimum pulse-width is 2 µsec.

Note: The external trigger mode can still be selected while the AWG is running. Therefore, an AWG can always be stopped, by selecting the "DISABLED" mode, even if an external trigger signal is continuously present.

6.2.8 Set AWG Clock-Period

For each of the two DAC-Boards (Lower, Higher) the "AWG Clock-Period" can be set. The same Clock-Period is used for AWG-A and AWG-B on the Lower DAC-Board respective AWG-C and AWG-D on the Higher DAC-Board. Its range is from 10 µsec to 4E9 µsec (corresponding to 1.111 hours). The default value is 10 µsec:

Note 1: The "AWG Clock Period" can be changed while the AWG is running. This allows the AWG-Frequency to be changed on the fly while the AWG is running continuously.

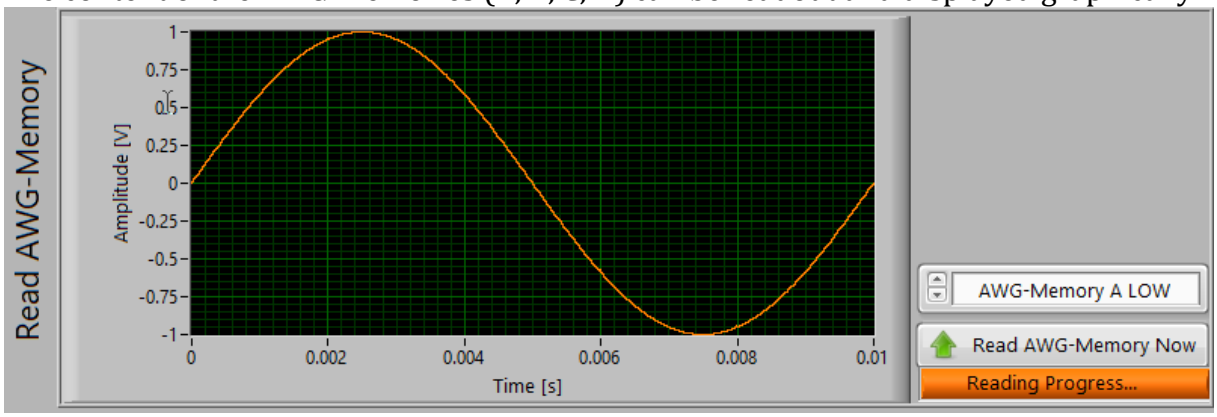
Note 2: When a waveform is generated by using the "Tab 4 | Standard Waveform Generation" with the option "Adapt AWG-CLK" set – and then written to the AWG-Memory – the corresponding "AWG Clock Period" gets automatically updated to meet the desired AWG frequency. See also chapter "Standard Waveform Generation".

6.2.9 AWG 1 MHz CLK Output OFF/ON

The AWG 1 MHz Reference Clock output signal can be used for time-synchronization with other devices. It is available on pin 14 of the D-SUB 25-pin connector on the back panel. By default, it is switched OFF to minimize the power consumption and the crosstalk to the other digital signals on the same connector.
The AWG 1 MHz Reference Clock is internally used for the clock generation of the four AWGs.

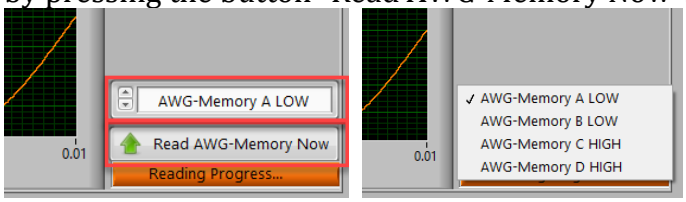
6.3 Read AWG-Memory

The content of the AWG-Memories (A, B, C, D) can be readout and displayed graphically:



The x-axis is "Time [s]"; its full-range is calculated by the "Clock-Period" times the "AWG Memory Size". The y-axis is the "Amplitude [V]" calculated directly from the readout AWG data; no reverse-linearization gets applied.

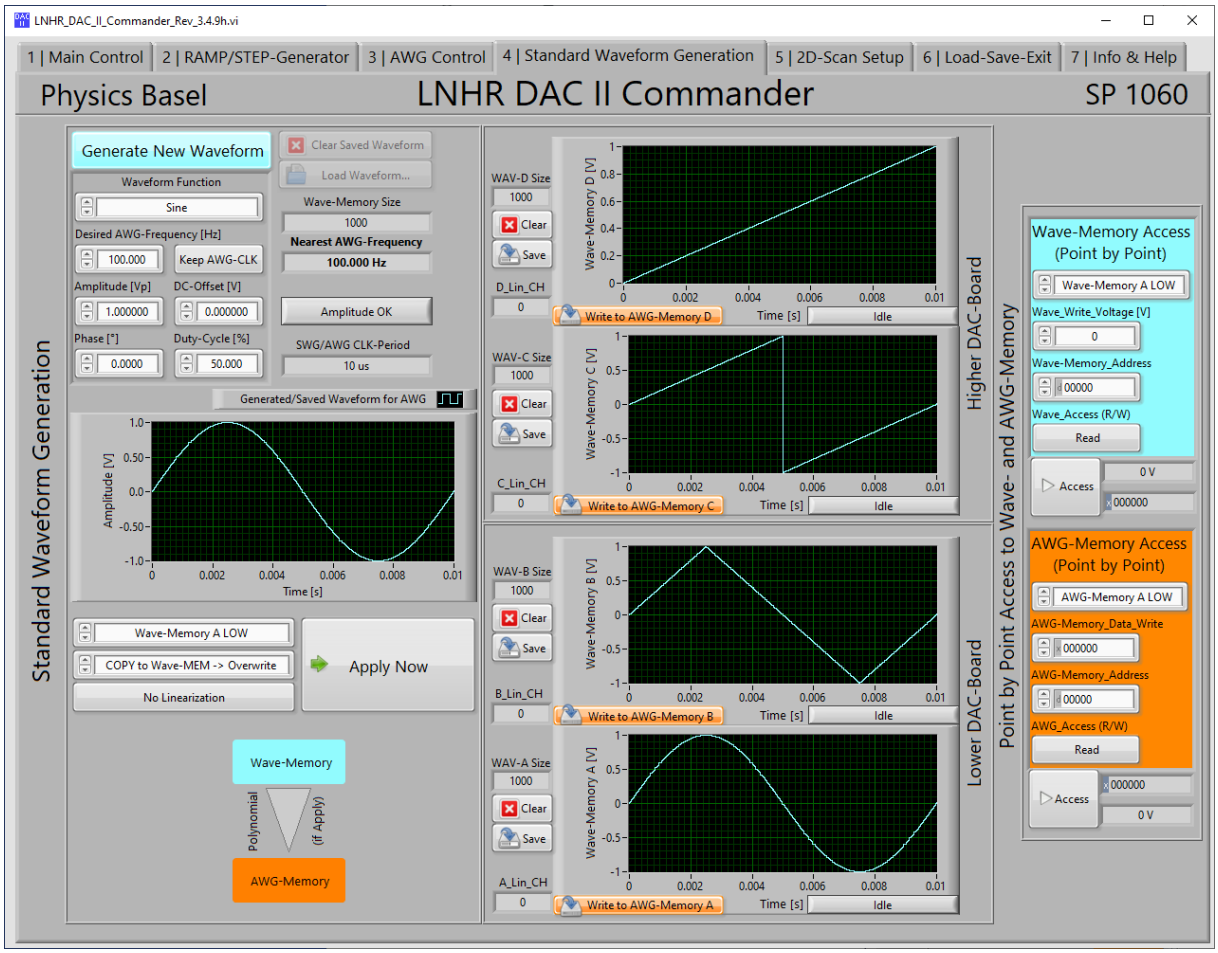
The AWG-Memory (A, B, C, D) to be readout can be selected here and the read is started by pressing the button "Read AWG-Memory Now":



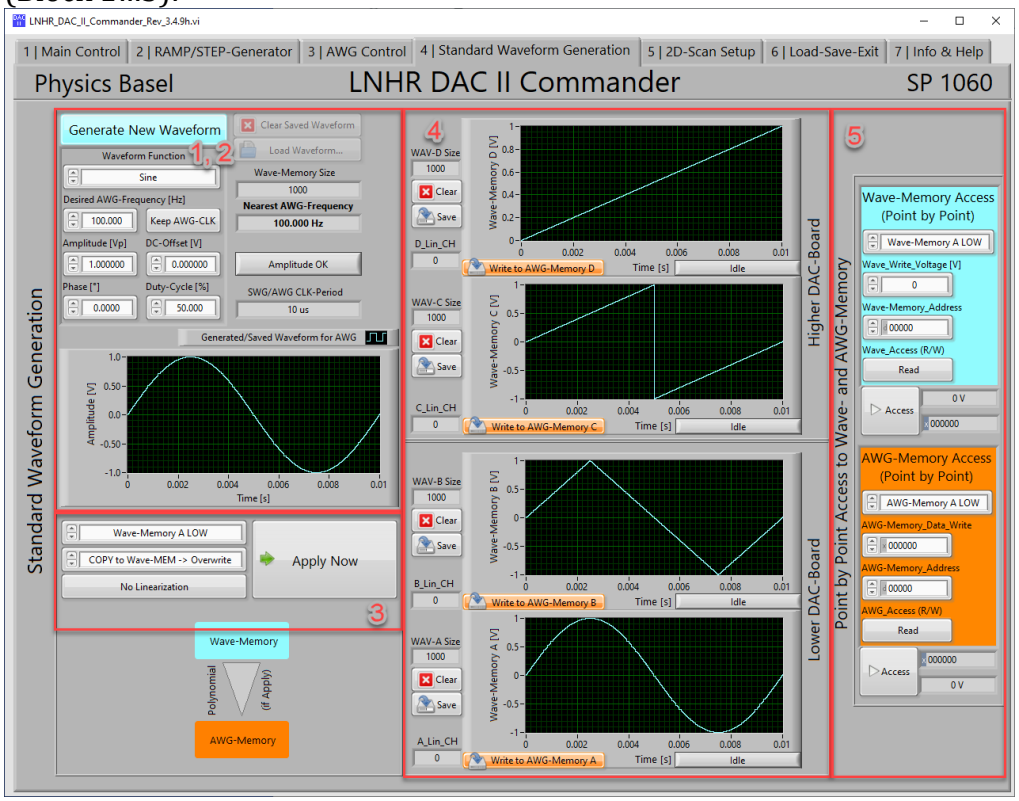
The readout is done for the points given in the parameter "AWG Memory Size" – in this example the AWG-A has a size of 1'000 points and the readout is performed from the AWG address 0 to 999.

Reading out the AWG memory with the maximum size of 34'000 points takes about 3 seconds - see the "Reading progress..." bar during the reading process.

7 Tab 4 | Standard Waveform Generation

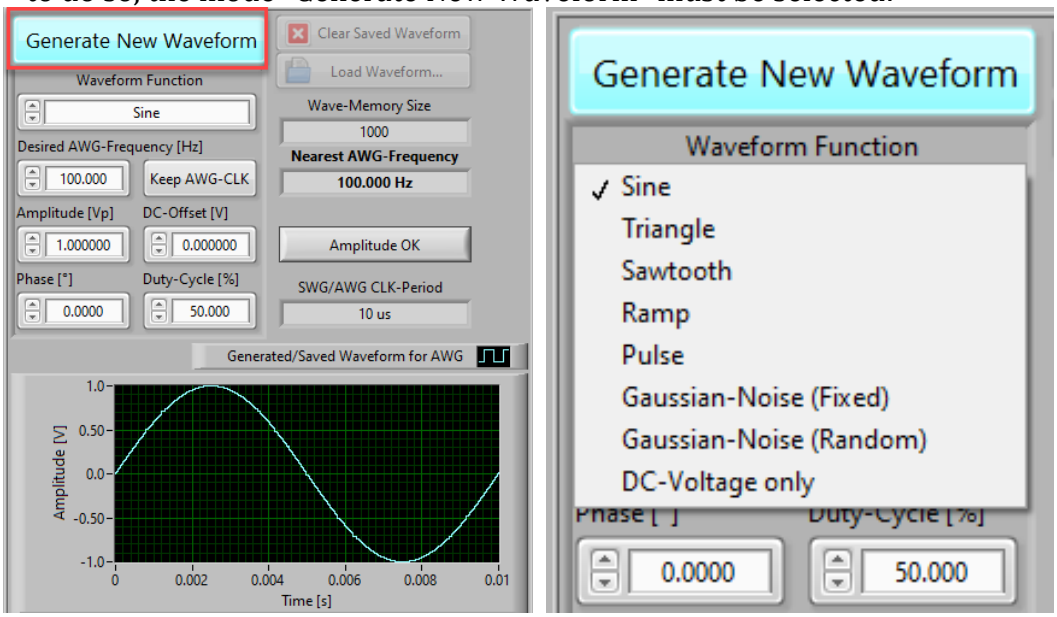


Tab 4 “Standard Waveform Generation” can be subdivided into the following five Blocks (Block 1…5):



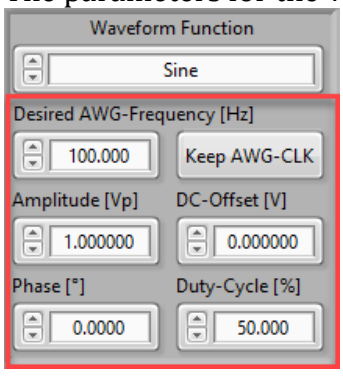
7.1 Block 1: Generate New Waveform

Here you can generate a new waveform base on several standard "Waveform Functions" – to do so, the mode "Generate New Waveform" must be selected:



Eight different "Waveform Functions" can be selected:
0 = Sine function – for a Cosine function select a Phase [°] of 90°
1 = Triangle function
2 = Sawtooth function
3 = Ramp function
4 = Pulse function – the parameter Duty-Cycle [%] is applied
5 = Gaussian Noise (Fixed) – always the same seed for the random/noise-generator
6 = Gaussian Noise (Random) – random seed for the random/noise-generator
7 = DC-Voltage only – a fixed voltage is generated

The parameters for the Waveform Generation can be specified in these fields:



Note: As soon as you update one parameter and press ENTER or leaving the control field with the mouse, the new waveform is automatically generated.

7.1.1 Desired AWG-Frequency [Hz]

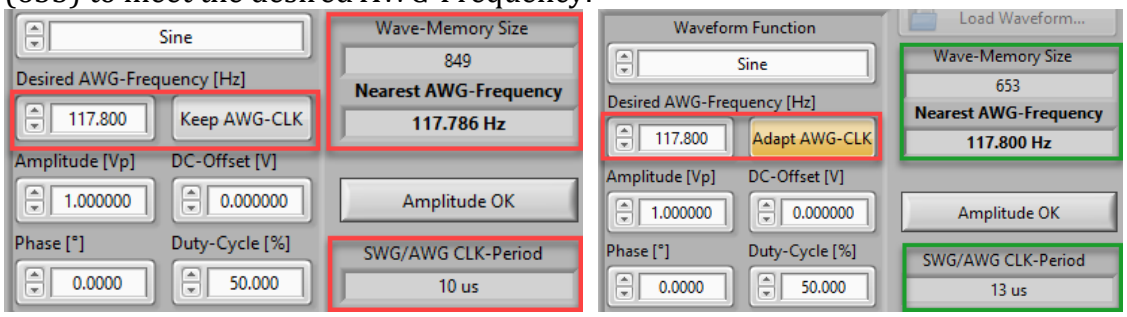
The "Desired AWG-Frequency [Hz]" can be set in the range between 0.001 Hz and 10'000 Hz; at the maximum frequency of 10 kHz only ten (10) sample points per period are available. Sometimes it isn't possible to reach exact the "Desired AWG-Frequency [Hz]" with the given "SWG/AWG Clock-Period".

Since the "Gaussian Noise" and the "DC-Voltage only" have no frequency, the parameter "Desired AWG-Frequency [Hz]" is used to define the "Wave-Memory Size" where the noise or the constant voltage is created.

7.1.2 Keep AWG-CLK / Adapt AWG-CLK 

If "Keep AWG-CLK" is selected, the set "AWG-Clock-Period" in "Tab 3 | AWG Control" is used as "SWG/AWG Clock-Period". At the default "AWG-Clock-Period" of 10 µsec the minimal possible AWG-Frequency of 2.941 Hz is given by the maximum AWG-Memory Size of 34'000 points.
For a "Desired AWG-Frequency [Hz]" smaller than 2.941 Hz the "Adapt AWG-CLK" must be selected.
If "Adapt AWG-CLK" is selected the "SWG/AWG Clock-Period" and the "Wave-Memory Size" is automatically adapted to reach the disered AWG-Frequency as close as possible.

In the example below a "Desired AWG-Frequency [Hz]" of 117.8 Hz is given. If "Keep AWG CLK" is selected a "Nearest AWG-Frequency" of 177.786 Hz can be reached, since the default "SWG/AWG Clock-Period" of 10 µsec is fixed. If "Adapt AWG-CLK" is selected the exact "Desired AWG-Frequency [Hz]" of 117.8 Hz is reached, since the algorithm can optimally adapt the "SWG/AWG Clock-Period" (13 µsec) and the "Wave-Memory Size" (653) to meet the desired AWG-Frequency:



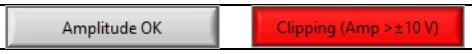
Note: If "Adapt AWG-CLK" is set, the frequency of second AWG-Channel may be affected, since the same "AWG Clock-Period" is used for both AWG-Channels of one DAC-Board.

7.1.3 Amplitude [Vp]

The "Amplitude [Vp]" defines the peak-voltage of the generated Standard Waveform. For Gaussian-Noise the "Amplitude [Vp]" corresponds to the RMS-value which is standard deviation (sigma).
The "Amplitude [Vp]" can be set within the range from -50.000000 V and +50.000000 V. The ±50 V range extends the flexibility in generating clipping-waveforms, also by applying a DC-Offset Voltage. A negative "Amplitude [Vp]" corresponds to a shift in "Phase [°]" of 180° (inverted function).

7.1.4 DC-Offset [V]

The "DC-Offset [V]" is added to the function and therefore shifts the waveform in the amplitude. If "DC-Voltage only" is selected as function, this parameter is used as fixed DC-Voltage. The range of the "DC-Offset [V]" is from -10.000000 V to +10.000000 V.

7.1.5 Amplitude OK / Clipping (Amp > ±10 V) 

If the amplitude of the generated waveform is always within the ± 10 V range, the "Amplitude OK" is displayed.

In case the amplitude of the generated waveform exceeds anywhere the maximum voltage range of ± 10 V, the warning "Clipping (Amp > ±10 V)" is displayed. However, even such to ±10 V truncated waveform can be still used.

7.1.6 Phase [°]

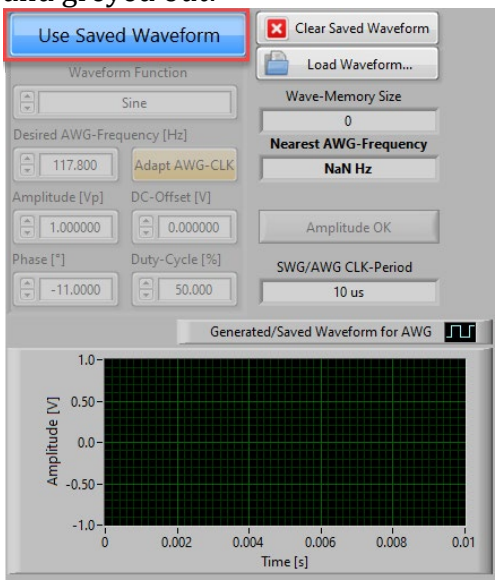
The "Phase [°]" shifts the generated waveform in the horizontal axis (time); a full period corresponds to 360°. The parameter "Phase [°]" isn't applicable for "Gaussian-Noise", "Ramp" and "DC-Voltage only" – for these "Waveform Functions" it is ignored.
A Sine-Wave with a "Phase [°]" of 90° corresponds to a Cosine-Wave. The "Phase [°]" can be set between -360.0000° and +360.0000.

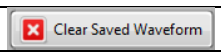
7.1.7 Duty-Cycle [%]

The "Duty-Cycle [%]" is only applicable for the Pulse function; for all other "Waveform Functions" this parameter is ignored.
A 50% Duty-Cycle results in a Square Wave; the higher the "Duty-Cycle [%]" the longer a high-level is applied. The "Duty-Cycle [%]" can be set between 0.000% and 100.000%.

7.2 Block 2: Use Saved Waveform / Load Waveform…

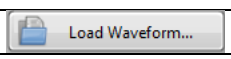
When selecting "Use Saved Waveform" a previously "Saved Waveform" can be recalled – for saving a waveform, see the description of Block 3 of this chapter. This feature allows to duplicate the same waveform to multiple AWG channels.
In the mode "Use Saved Waveform" the controls for the waveform generation are disabled and greyed out:



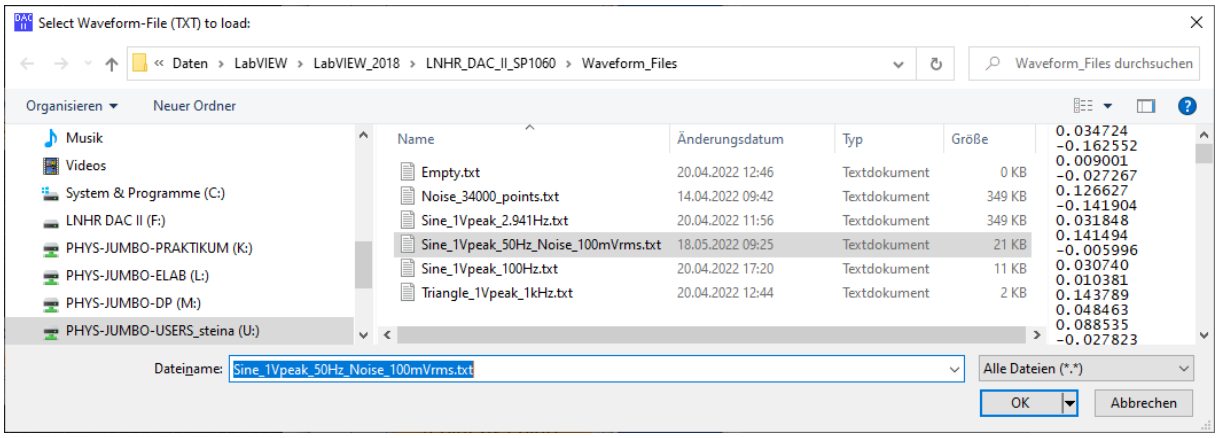
7.2.1 Clear Saved Waveform 

The previously "Saved Waveform" can be cleared by pressing the button "Clear Saved Waveform" – then the "Wave-Memory Size" is reset to zero (0).

Note: For optimal system performance, always clear unused Wave-Memories.

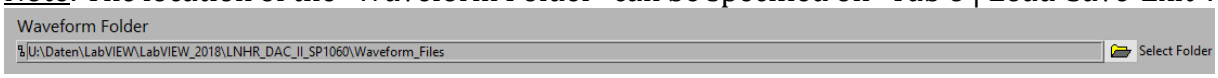
7.2.2 Load Waveform… 

When pressing the button "Load Waveform…" a new window with the title "Select Waveform-File (TXT) to load:" appears:

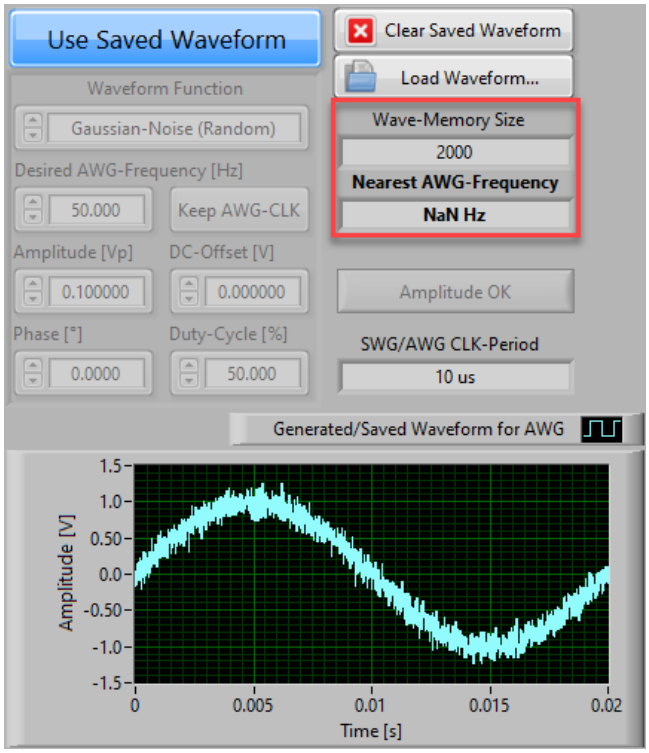


Here you can select the Waveform-File which shall be loaded into the Saved Waveform memory of the LNHR DAC II. A Waveform-File is a simple text file that contains floating-point numbers in a column; the columns are separated by a carriage-return. The user can edit such a Waveform-File with a simple text editor or they can be generated by other software tools.
Further, the generated Wave-Memories can also be saved as Waveform-Files in such a text format – see the description of Block 3 of this chapter.

Note: The location of the "Waveform Folder" can be specified on "Tab 6 | Load-Save-Exit":



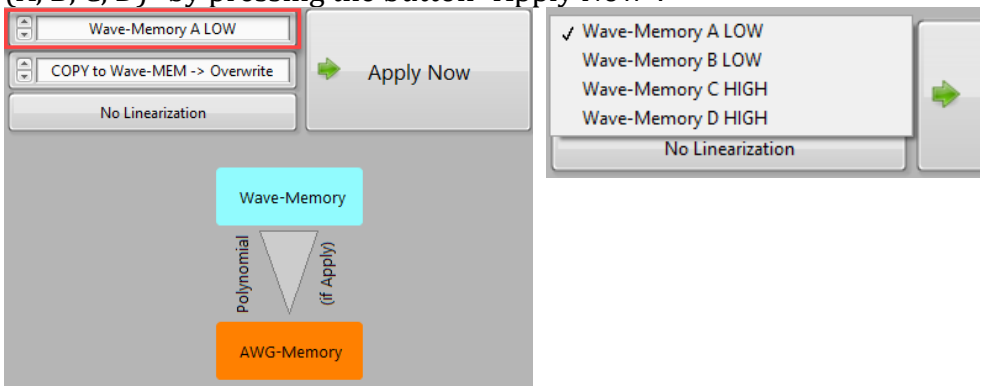
In this example the Waveform-File "Sine_1Vpeak_50Hz_Noise_100mVrms.txt" is loaded; this is a 50 Hz / 1 Vp Sinewave with 100 mVrms of Gaussian-Noise and is then displayed as "Saved Waveform":



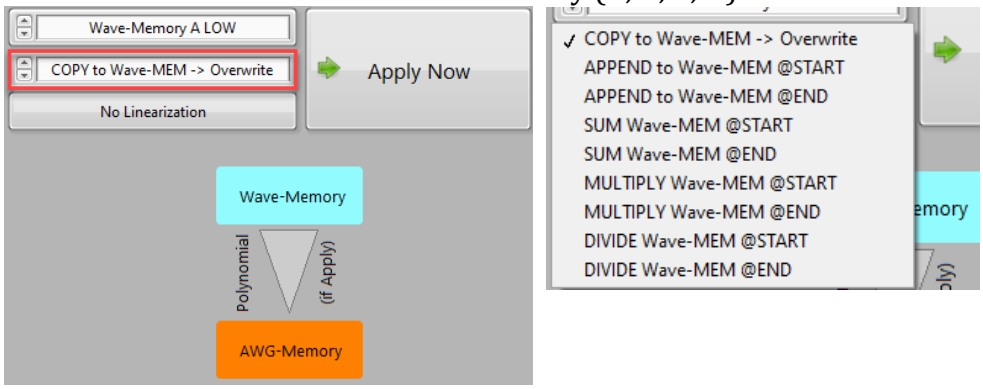
The "Wave-Memory Size" is updated (in this example 2'000) and the "Nearest AWG-Frequency" is given as "NaN" since this is unclear from a loaded/saved waveform.

7.3 Block 3: Waveform to Wave-Memory

Here the generated or loaded waveform can be transferred to the selected "Wave-Memory (A, B, C, D)" by pressing the button "Apply Now":



One of these "Wave-Functions" can be selected to be applied when the waveform is transferred to the selected "Wave-Memory (A, B, C, D)":



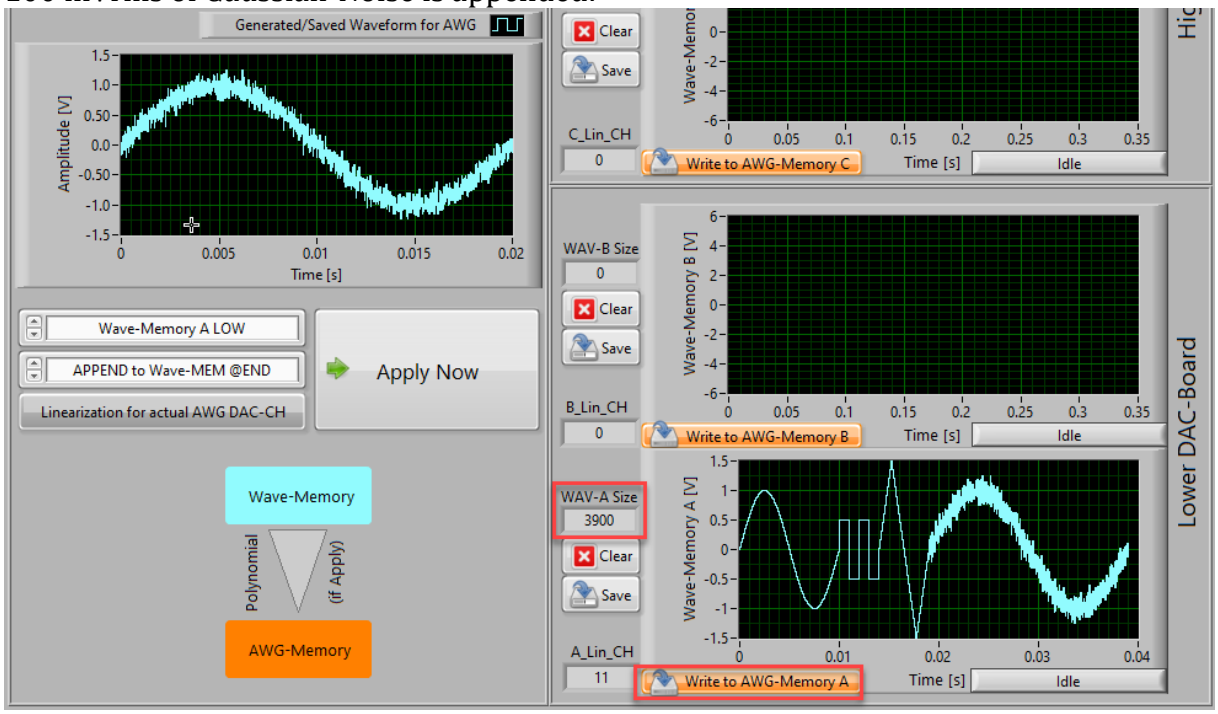
The following nine different "Wave-Functions" available:
0 = COPY to Wave-Memory-> Overwrite
1 = APPEND to Wave-Memory @START
2 = APPEND to Wave-Memory @END
3 = SUM Wave-Memory @START
4 = SUM Wave-Memory @END
5 = MULTIPLY Wave-Memory @START
6 = MULTIPLY Wave-Memory @END
7 = DIVIDE Wave-Memory @START
8 = DIVIDE Wave-Memory @END

When "COPY to Wave-MEM" is selected, the selected "Wave-Memory" is overwritten. The other four "Wave-Functions" COPY, APPEND, SUM, MULTIPLY and DIVIDE can be applied to START or to the END of the selected "Wave-Memory".

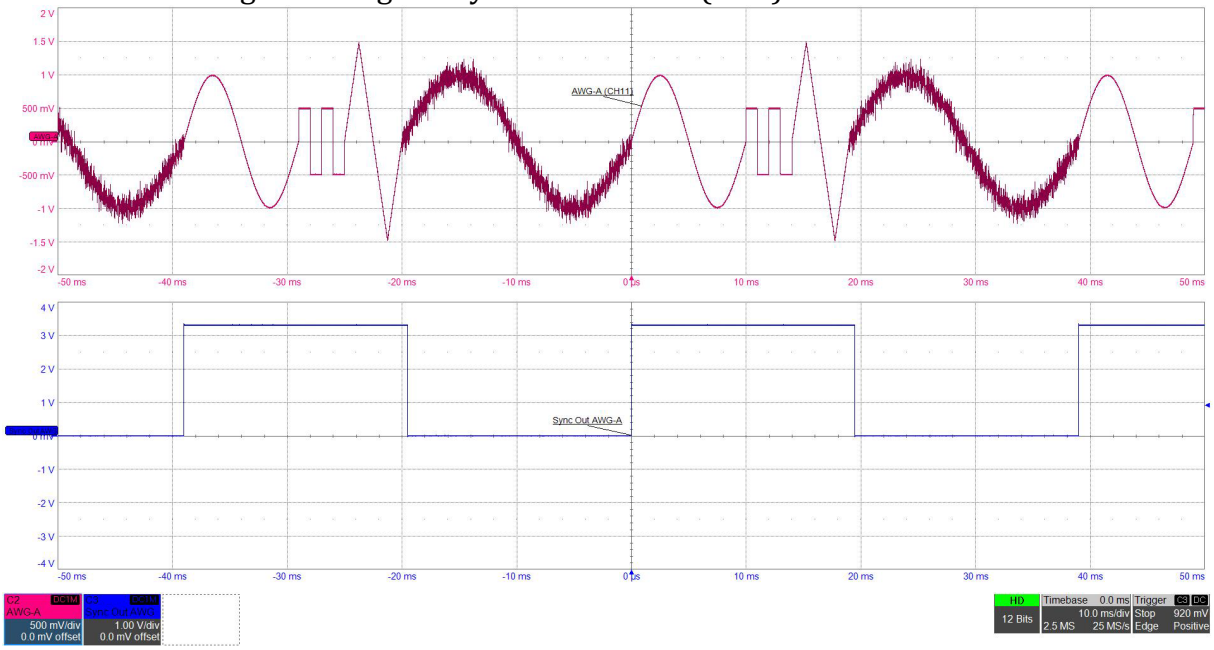
With these nine different "Wave-Functions" complex and user-specific waveforms can be created in the "Wave-Memory (A, B, C, D)". Multiple "Wave-Functions" can be applied on different generated Standard Waveforms to reach the desired user-specific waveform.

In the example below the waveform of "Wave-Memory A" is composed by appending four different waveforms: First a single cycle 100 Hz / 1 Vp Sinewave is generated, then two cycles of a 500 Hz / 0.5 Vp Square-Wave are appended, then a single cycle Triangle-Wave

with 200 Hz / 1.5 Vpeak is appended and at last the loaded a 50 Hz / 1 Vp Sinewave with 100 mVrms of Gaussian-Noise is appended:



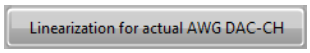
This composed waveform consists of 3'900 points which shown in the indicator "WAV-A Size"; at an "AWG Clock-Period" of 10 µsec the duration is therefore 39 msec.
By pressing the button "Write to AWG-Memory A" this waveform is copied to the AWG-Memory A. Now the AWG-A can be started; do not forget to turn ON the corresponding DAC-Channel with HBW (100 kHz). If "AWG Cycles (0=Inf)" is set to zero (0) the composed waveform is output repetitively. The upper grid shows the AWG-A (CH11) output (red) and on the lower grid the signal "Sync Out AWG-A" (blue):



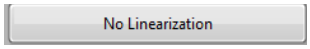
The "Sync Out AWG-A" is high for the first 50% of the AWG points (3'900); at an "AWG Clock-Period" of 10 µsec this 1'950 AWG points (Sync Out high) corresponds to a duration of 19.5 msec.

7.3.1 No Linearization / Linearization for actual AWG DAC-CH

This control determines whether the linearization should be applied later when the Wave-Memory is written to the AWG Memory.



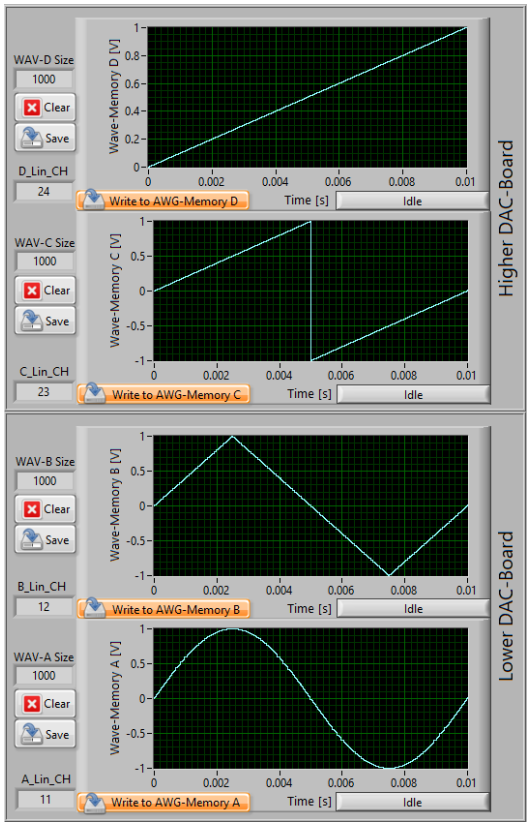
If "Linearization for actual DAC-CH" is set, the AWG DAC-Channel selected on Tab 3 gets registered when the "Wave-Function" is applied ("Apply Now" pressed). This DAC-Channel is later used for the linearization when the Wave- Memory is written to the AWG Memory. This option results in a minimal AWG signal distortion, since the linearization coefficients of this specific DAC-Channel are applied. However, you should not later change the DAC-Channel that is mapped to the corresponding AWG channel (A, B, C, D).



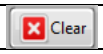
If "No Linearization" is selected the DAC-Channel is registered as zero (0) and therefore no linearization will be applied later when the Wave- Memory is written to the AWG Memory. This option results in more AWG signal distortion; but then you can later change the DAC channel that is mapped to the corresponding AWG channel (A, B, C, D).

7.4 Block 4: Wave-Memories Overview & Write to AWG-Memories

Here you have the overview on the four "Wave-Memories". On bottom the two "Wave-Memories (A, B)" related to the AWG-A and AWG-B on the Lower DAC-Board are shown. On top the two "Wave-Memories (C, D)" related to the AWG-C and AWG-D on the Higher DAC-Board are indicated:



For each of the four "Wave-Memories" the registered linearization DAC-Channel is displayed in the field "A, B, C, D Lin_CH"; if "No Linearization" was selected this number is zero (0). Further, the size of the "Wave-Memories" is shown in the indicator "WAV-A, B, C, D Size"; the range is from 0 to 34'000.

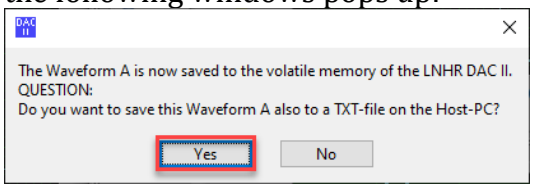
7.4.1 Clear Wave-Memory 

Each of the four "Wave-Memories" can be individually cleared by pressing the button "Clear" – then the "WAV Size" is reset to zero (0).

Note: For optimal system performance, always clear unused Wave-Memories.

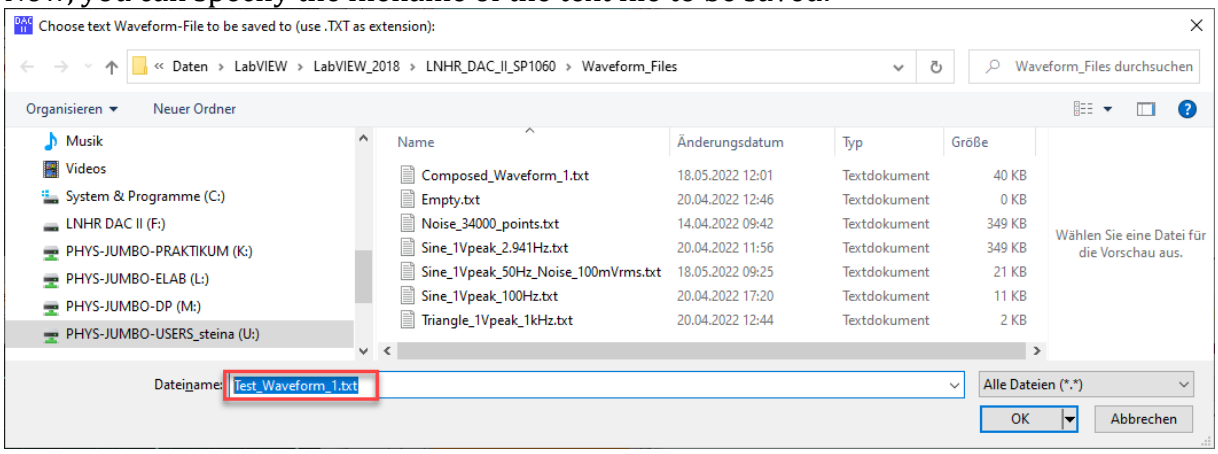
7.4.2 Save Wave-Memory 

When pressing this button, the waveform of the corresponding "Wave-Memory" is immediately saved to the internal volatile memory of the LNHR DAC II. Only one waveform can be stored in this internal volatile memory at the same time. This saved waveform can be retrieved when the "Use Saved Waveform" is selected – see description of Block 2 in this chapter.
After the waveform has been saved to the internal volatile memory of the LNHR DAC II the following windows pops up:



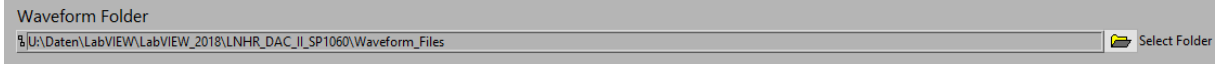
If you press "Yes" you can save this waveform also to a non-volatile text file on the host PC. This way you can later load this waveform by using "Load Waveform…" when "Use Saved Waveform" is selected – see description of Block 2 in this chapter.

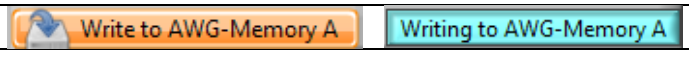
Now, you can specify the filename of the text file to be saved:



A short message indicates that the waveform text file has successfully been saved.

Note: The location of the "Waveform Folder" can be specified on "Tab 6 | Load-Save-Exit":

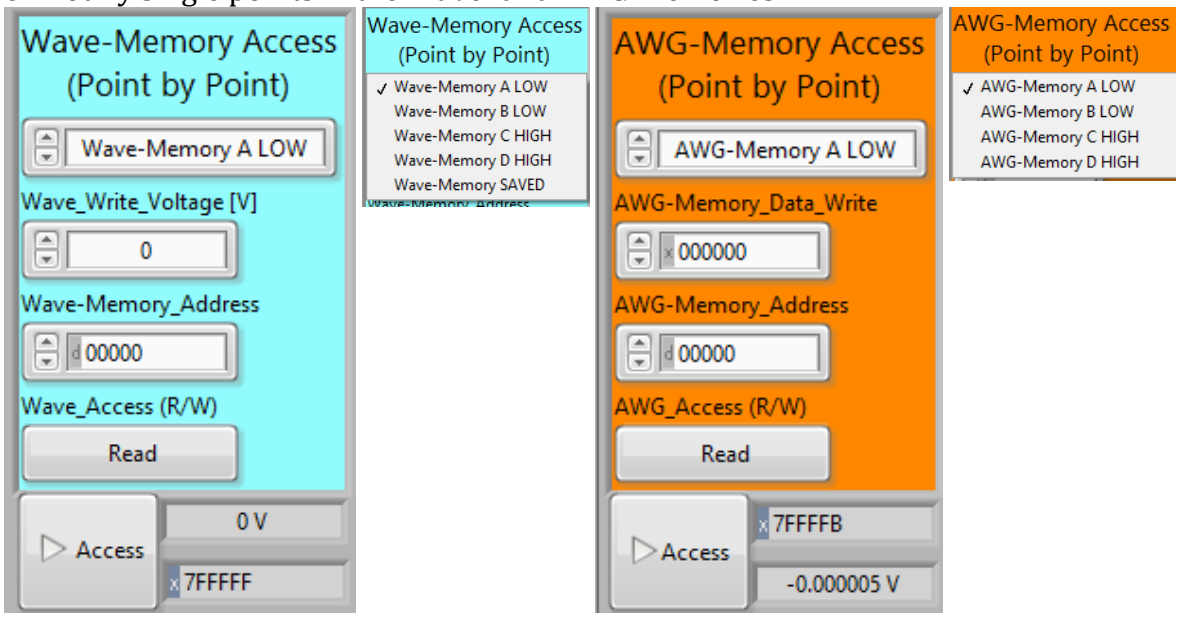


7.4.3 Write to AWG-Memory 

When pressing this button, the waveform of the "Wave-Memory A, B, C, D" is written to the corresponding "AWG-Memory A, B, C, D". Now the linearization for the registered DAC-Channel is performed; if the registered DAC-Channel is zero (0) no linearization is done. Writing a waveform of the maximum size of 34'000 points takes around three (3) seconds – during this time the indicator changes from "Idle" to "Writing to AWG-Memory".

7.5 Block 5: Point by Point Access to Wave- and AWG-Memories

The "Wave-Memory A, B, C, D, SAVED" as well as the "AWG-Memory A, B, C, D" can be accessed point by point (Address 0…33'999) by the user. This feature can be used to check of modify single points in the Wave- and AWG-Memories:

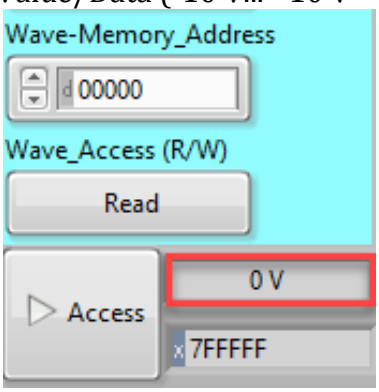


In the example above the "Wave-Memory A LOW" as well as the "AWG-Memory A LOW" are readout at the same "Wave-Memory Address" of zero (0). The Wave-Memory reads 0x7FFFFF (0 V) while the AWG-Memory reads 0x7FFFFB (-0.000005 V). This discrepancy comes from the fact that the linearization for DAC-Channel 11 was applied when the Wave-Memory was written to the AWG-Memory. If "No Linearization" had been selected, the same values would be read from both memories.

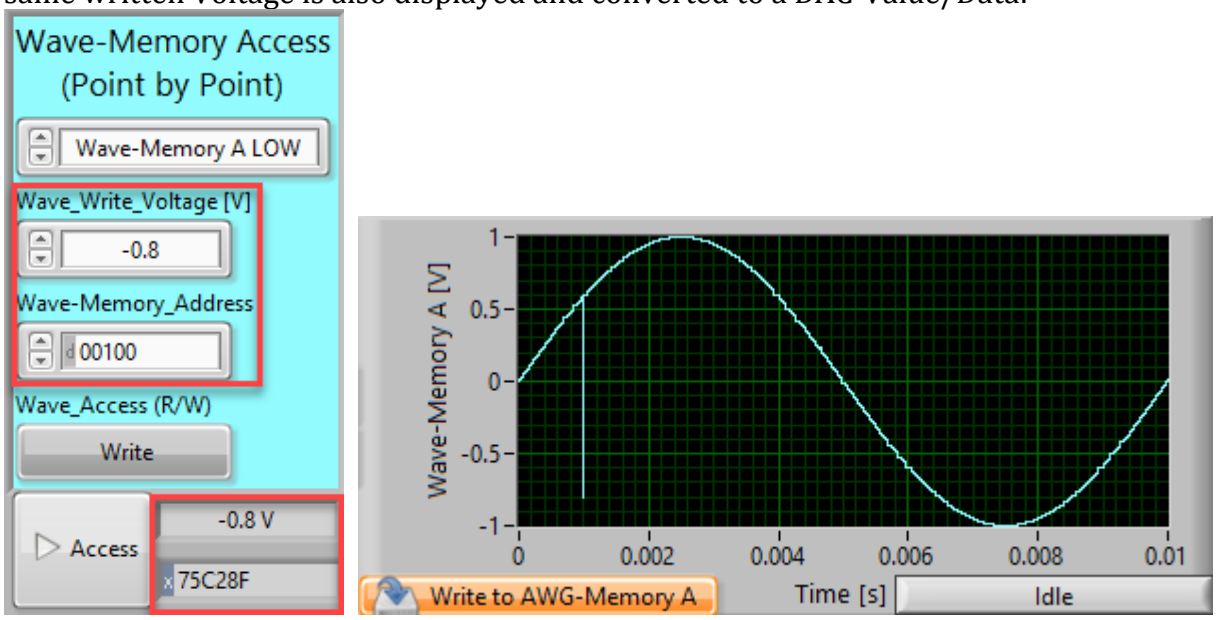
The point by point access to the Wave-Memory is possible for the four normal Wave-Memories (A, B, C, D) and also for the SAVED-Memory; all these waveforms are stored in the volatile memory of the LNHR DAC II.

7.5.1 Wave-Memory Read / Write Access

Accessing the Wave-Memory can be either in "Read" or "Write" mode. When reading from a Wave-Memory the control "Wave Write Voltage [V]" is ignored. The readout is done when the button "Access" is pressed. Then the Voltage (±10 V) at the specified decimal "Wave-Memory Address" (0…33'999) is readout; the Voltage is also converted to a DAC-Value/Data (-10 V... +10 V => HEX 0x00000... 0xFFFFF):



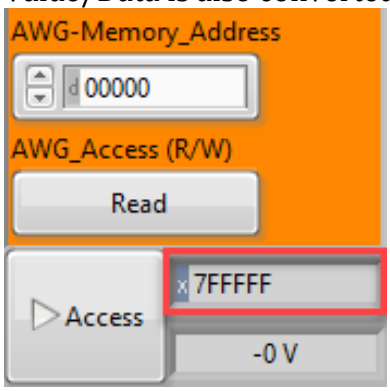
In the "Write" mode, the value given in "Wave Write Voltage [V]" is written at the specified decimal "Wave-Memory Address" (0…33'999) when the button "Access" is pressed. The same written Voltage is also displayed and converted to a DAC-Value/Data:



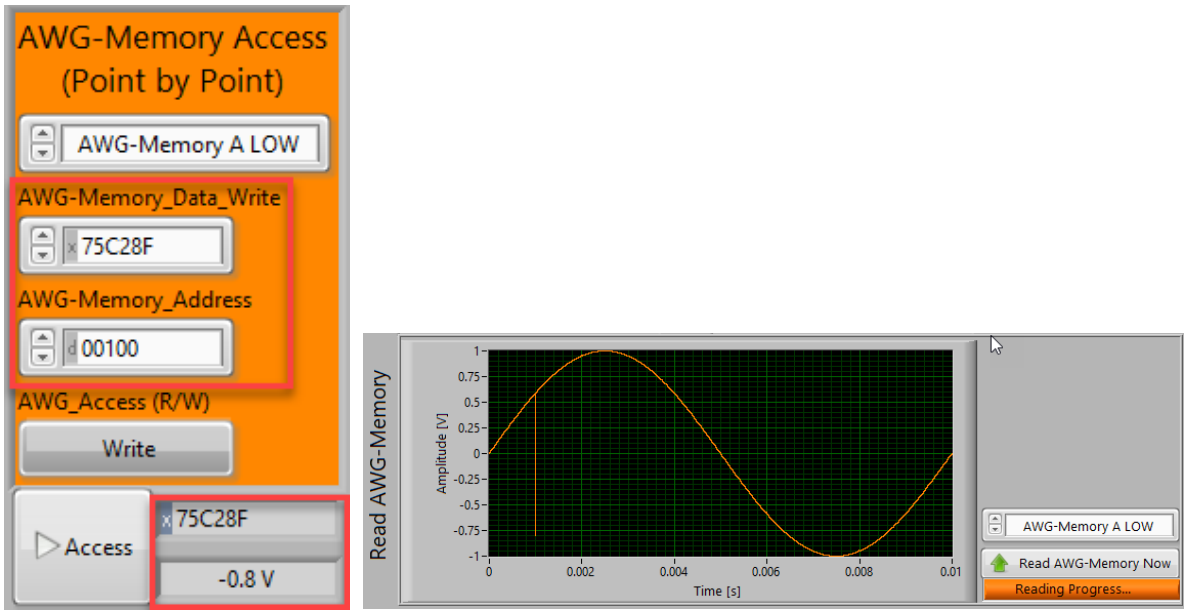
In the example above, on the "Wave-Memory A LOW" a new voltage of -0.8 V ("Wave Write Voltage [V]") at the "Wave-Memory Address" of 100 (decimal) is written. Pressing the "Access" button, writes this new voltage and also immediately updates the "Wave-Memory A [V]" graph.

7.5.2 AWG-Memory Read / Write Access

Accessing the AWG-Memory can be either in "Read" or "Write" mode. When reading from an AWG-Memory the control "AWG-Memory Data Write" is ignored. The readout is done when the button "Access" is pressed. Then the DAC-Value/Data (HEX 0x00000... 0xFFFFF) at the specified decimal "AWG-Memory Address" (0…33'999) is readout; the DAC-Value/Data is also converted to a Voltage (HEX 0x00000... 0xFFFFF => -10 V... +10 V):



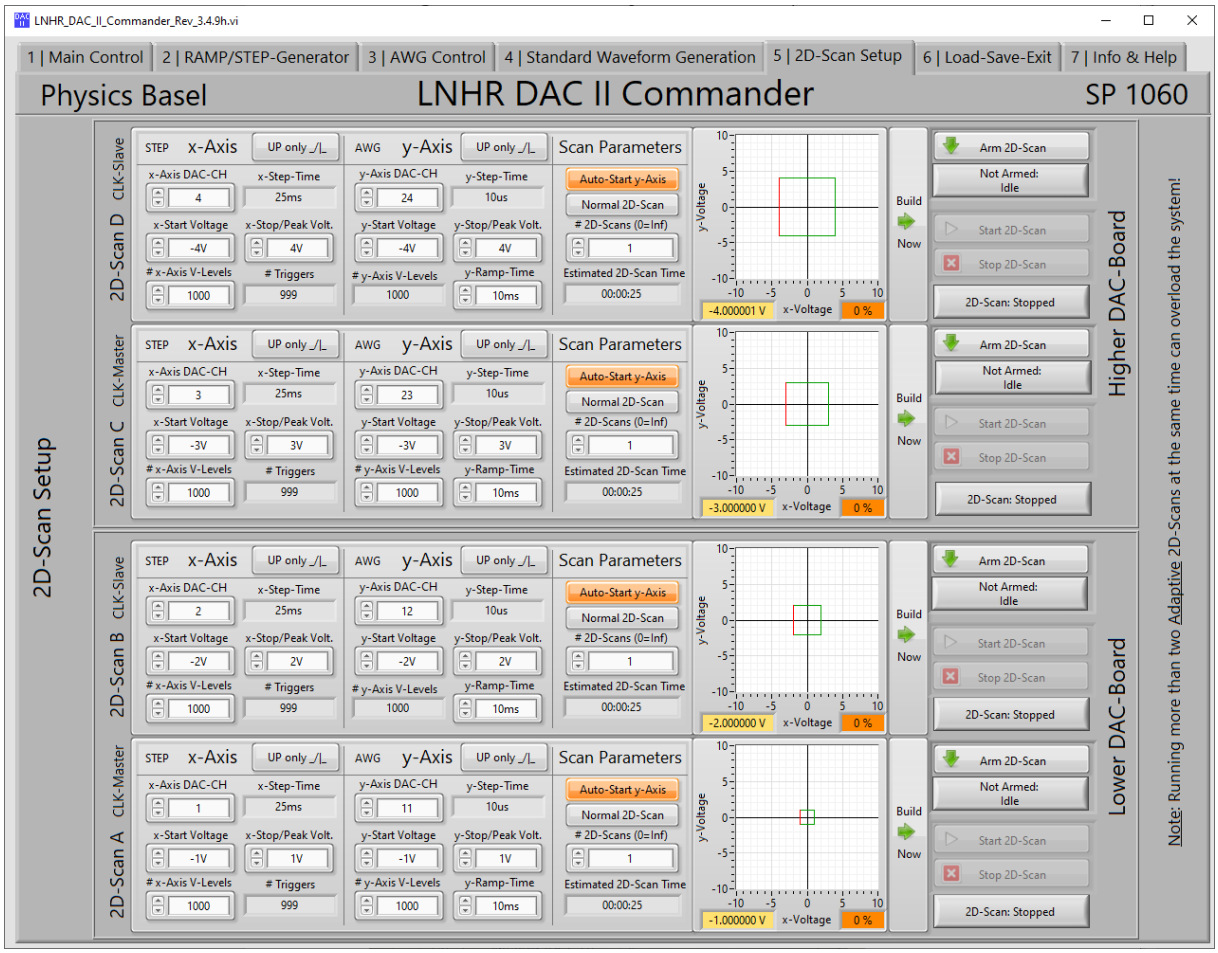
In the "Write" mode, the value given in "AWG-Memory Data Write" is written at the specified decimal "AWG-Memory Address" (0…33'999) when the button "Access" is pressed. The same written DAC-Value/Data is also displayed and converted to a Voltage:



In the example above, on the "AWG-Memory A LOW" a new DAC-Value/Data of 0x75C28F ("AWG-Memory Data Write") at the "AWG-Memory Address" of 100 (decimal) is written. Pressing the "Access" button, writes this new DAC-Value/Data which corresponds to a Voltage of -0.8 V. When the "AWG-Memory A LOW" is readout on the "Tab 3 | AWG Control" the new value is indicated on the "Read AWG-Memory" graph (see above).

Note: Writing point by point directly to AWG-Memories doesn't involve a linearization.

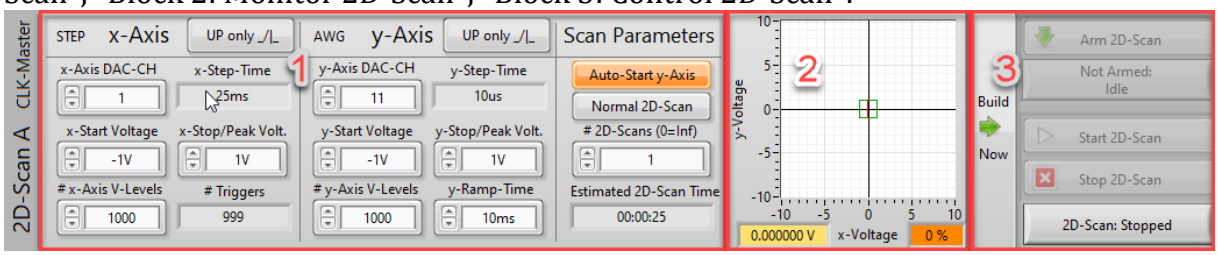
8 Tab 5 | 2D-Scan Setup



On this "Tab 5 | 2D-Scan Setup" the four 2D-Scans can be generated, monitored and controlled. Setting up a new 2D-Scan is user-friendly and intuitive. Such a 2D-Scan is automatically built by programming and accessing the STEP-Generator (Tab 2), the AWG Control (Tab 3) and the Standard Waveform Generation (Tab 4).

Note: Since this "2D-Scan Setup" feature is coded in the "LNHR DAC II Commander" application, it cannot be accessed via remote control commands to the LNHR DAC II. However, such a 2D-Scan can also be generated by a larger sequence of remote-control commands.

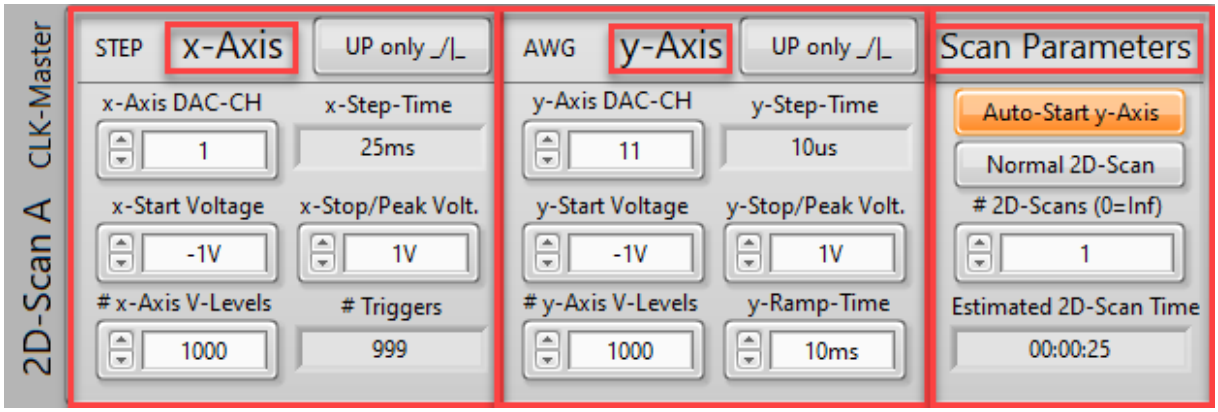
Tab 5 "2D-Scan Setup" can be divided into the following three Blocks: "Block 1: Setup 2D-Scan"; "Block 2: Monitor 2D-Scan"; "Block 3: Control 2D-Scan":



Note: Avoid overloading the device by sending a large number of remote commands while running 2D-Scans in Auto-Start mode. Otherwise, the 2-Scan can be interrupted.

8.1 Block 1: Setup 2D-Scan

The “Setup 2D-Scan” can be structured in the three groups “2D-Scan x-Axis”, “2D-Scan y-Axis” and “2D-Scan Parameters”:



8.1.1 2D-Scan x-Axis

In this part the parameters of the x-axis of the “2D-Scan” are defined. The “x-Axis” is generated by using the STEP-Generator – see chapter “Tab 2 | RAMP/STEP-Generator”.

8.1.1.1.1 Up only / UP-DOWN

This parameter defines the shape of the “x-Axis” during a 2D-Scan. If “UP only” is selected, the x-axis voltage goes from “x-Start Voltage” to “x-Stop/Peak Voltage”; this corresponds to one complete 2D-Scan.
If “UP-DOWN” is selected, the x-axis voltage goes from “x-Start Voltage” to “x-Stop/Peak Volt.” and then back again to “x-Start Voltage”; this is one complete 2D-Scan.

8.1.1.1.2 x-Axis DAC-CH, x-Start Voltage, x-Stop/Peak Volt.

The DAC-Channel for the x-axis voltage output is defined in “x-Axis DAC-CH”. A valid DAC-Channel is in the range from 1 to 24.

The “x-Start Voltage” defines the x-axis voltage where the 2D-Scan will be started. The “x-Stop/Peak Volt.” defines the x-axis voltage where the 2D-Scan will stop (“Up only”) or reach its peak voltage (“UP-DOWN”). Both values must be within ±10 V.

8.1.1.1.3 # x-Axis V-Levels, # Triggers

The parameter “# x-Axis V-Levels” defines the number of voltage levels in the x-axis that are performed during a 2D-Scan. This value must be in a range from 10 to 20’000’000.

The indicator “# Triggers” shows how many times the y-axis will be triggered during a single 2D-Scan (# 2D-Scans = 1). This is depending on the shape of the “x-Axis” (“Up only” or “UP-DOWN”) – for a detailed description see chapter “Tab 2 | RAMP/STEP-Generator”.

8.1.1.1.4 x-Step-Time

The indicator “x-Step-Time” shows the approximated time between two x-axis steps, but only if “Auto-Start y-Axis” is selected. This time depends on the “y-Ramp-Time” and the selected mode “Normal 2D-Scan” or “Adaptive 2D-Scan”. In “Adaptive 2D-Scan” mode the “x-Step-Time” is increased because the reload of the AWG-Memory is time consuming. The “x-Step-Time” is calculated from the formulas in the chapter “Tab 2 | RAMP/STEP-Generator”.

If "Manual Start y-Axis" is selected, the time between two x-axis steps is defined by the user (external AWG-Trigger or trigger by a remote command or "Start 2D-Scan" pressed). Therefore, no meaningful "x-Step-Time" can be calculated and "NaNs" is displayed.

8.1.2 2D-Scan y-Axis

In this part the parameters of the y-axis of the "2D-Scan" are defined. The "y-Axis" is generated by using the AWG – see chapters "Tab 3 | AWG Control" and "Tab 4 | Standard Waveform Generation".

8.1.2.1.1 Up only / UP-DOWN

This parameter defines the shape of the "y-Axis" during a 2D-Scan. If "UP only" is selected, the y-axis voltage goes from "y-Start Voltage" to "y-Stop/Peak Voltage"; this corresponds to one complete y scan-line.
If "UP-DOWN" is selected, the y-axis voltage goes from "y-Start Voltage" to "y-Stop/Peak Volt." and then back again to "y-Start Voltage"; this is one complete y scan-line.

8.1.2.1.2 y-Axis DAC-CH, y-Start Voltage, y-Stop/Peak Volt.

The DAC-Channel for the y-axis voltage output is defined in "y-Axis DAC-CH". A valid DAC-Channel is in the range from 1 to 12 for the "2D-Scan A/B" running on the lower DAC-Board and from 13 to 24 for the "2D-Scan C/D" running on the higher DAC-Board.

The "y-Start Voltage" defines the y-axis voltage where the 2D-Scan will be started. The "y-Stop/Peak Volt." defines the y-axis voltage where the 2D-Scan will stop ("Up only") or reach its peak voltage ("UP-DOWN"). Both values must be within ±10 V.

8.1.2.1.3 # y-Axis V-Levels, y-Ramp-Time

The parameter "# y-Axis V-Levels" defines the number of voltage levels in the y-axis that are performed during a 2D-Scan; only on the Clock-Master 2D-Scans the "# y-Axis V-Levels" can be set. This value must be in a range from 10 to 15'000. If a short "y-Ramp-Time" is set, the "# y-Axis V-Levels" may be restricted to meet system requirements.

The "y-Ramp-Time" specifies the time for one complete y scan-line. The valid range is from 6 msec to 40'000 sec, which corresponds to around 11.1 hours.

8.1.2.1.4 y-Step-Time

The indicator "y-Step-Time" shows the time between two y-axis steps; this corresponds to the AWG Clock-Period which is common for both AWG channels on a DAC-Board. The "y-Step-Time" depends on the "# y-Axis V-Levels", the "y-Ramp-Time" and the shape of the "y-Axis" ("Up only" or "UP-DOWN"). The "y-Step-Time", which is equal to the AWG Clock-Period, can be between 10 µsec and 4'000 sec.

Note: The first 2D-Scan channel of each DAC-Board is the Clock-Master; the Clock-Masters are the "2D-Scan A" and the "2D-Scan C". The second 2D-Scan channel of each DAC-Board is the Clock-Slave; the Clock-Slaves are the "2D-Scan B" and the "2D-Scan D".

Clock-Master means, that this 2D-Scan controls the AWG Clock-Period which is common for both AWGs running on this DAC-Board. Thus, the y-Axis timing ("y-Ramp-Time" and "# y-Axis-Levels") of a Clock-Slave is dependent on the y-Axis timing of its Clock-Master. Therefore, the parameter "# y-Axis-Levels" of a Clock-Slave is not editable and set by its

Clock-Master. The "y-Ramp-Time" of a Clock-Slave can be set by the user, but can also be limited by its Clock-Master, if necessary. This happens when there is a large difference in "y-Ramp-Time" between the Clock-Master and the Clock-Slave.

8.1.3 2D-Scan Parameters

Here the parameters for the 2D-Scan are set and the estimated time for this specific 2D-Scan is calculated.

8.1.3.1.1 Manual Start y-Axis / Auto-Start y-Axis

If "Manual Start y-Axis" is selected, the user must start each y scan-line (AWG) by an external AWG-Trigger (TTL) or by a remote command or by pressing "Start 2D-Scan".

If "Auto-Start y-Axis" is selected, the next y scan-line (AWG) is automatically restarted when the x-Axis (STEP-Generator) has finished (time-delay = 5ms) – see chapter "Tab 2 | RAMP/STEP-Generator".

8.1.3.1.2 Normal 2D-Scan / Adaptive 2D-Scan

In "Normal 2D-Scan" mode, the same predefined AGW function (y-Axis) stays in the AWG-Memory. This scan mode is the fastest, but no adaption in y-Axis can be performed.

In "Adaptive 2D-Scan" mode, after each x-Step, the AWG-Memory is reloaded from the Wave-Memory by applying the Polynomial. A linear y-Adaption can be done with the parameter "Shift-Voltage [V/STP]" on Tab 2. For further information see chapter "Tab 2 | RAMP/STEP-Generator".

8.1.3.1.3 # 2D-Scans (0=Inf)

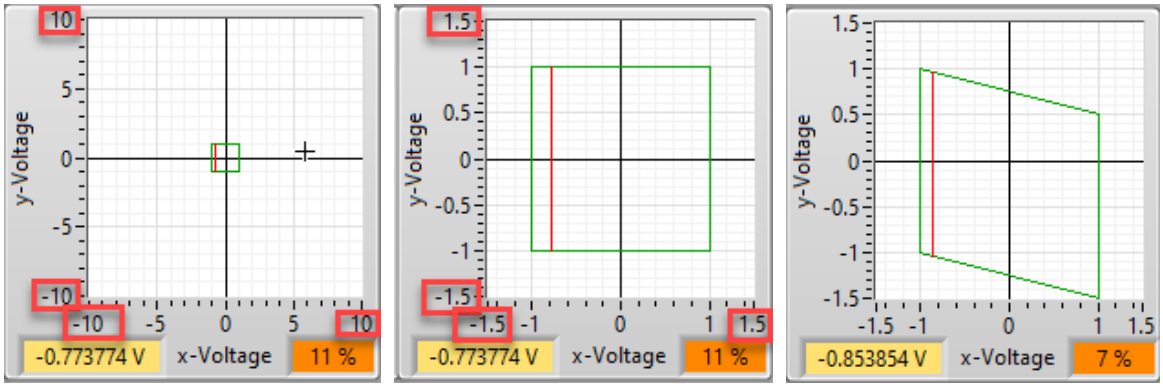
The number of complete 2D-Scans is defined with this parameter "# 2D-Scans (0=Inf)". The valid range is from 0 to 4E9. A value of zero (0) means that an infinite number of 2D-Scans are performed; then such a 2D-Scan must be stopped by the user.

8.1.3.1.4 Estimated 2D-Scan Time

The "Estimated 2D-Scan Time" indicates the time of a complete 2D-Scan in the format "hours:minutes:seconds" (hh:mm:ss). This time can only be estimated if "Auto-Start y-Axis" is selected and the numbers of the 2D-Scans is not zero (0 = running infinitely).

8.2 Block 2: Monitor 2D-Scan

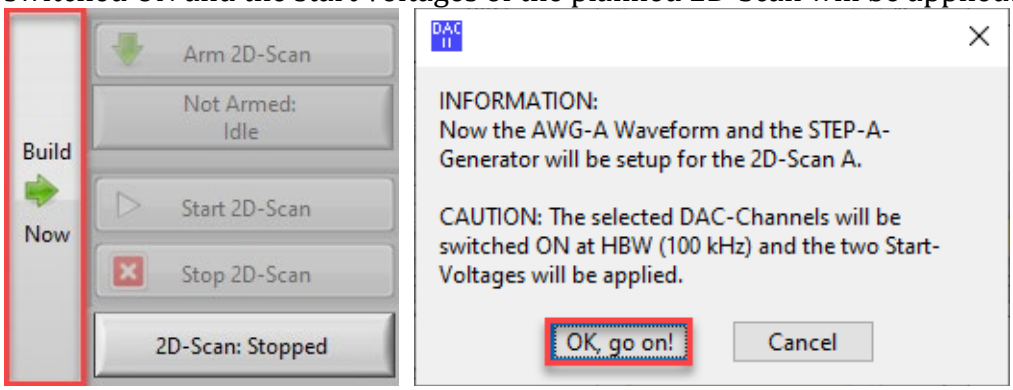
The defined 2D-Scan area is shown on the x/y-voltage graph as green rectangular (no adaption) or as rhombus (with y-adaption). You can zoom into the graph by editing the scale-numbers:



During a running 2D-Scan the actual x-voltage is indicated by a red line and its value is shown in the bottom left. Further the percentage [%] of the 2D-Scan done is indicated in the bottom left. The graph on the right shows an adaptive 2D-Scan (rhombus).

8.3 Block 3: Control 2D-Scan

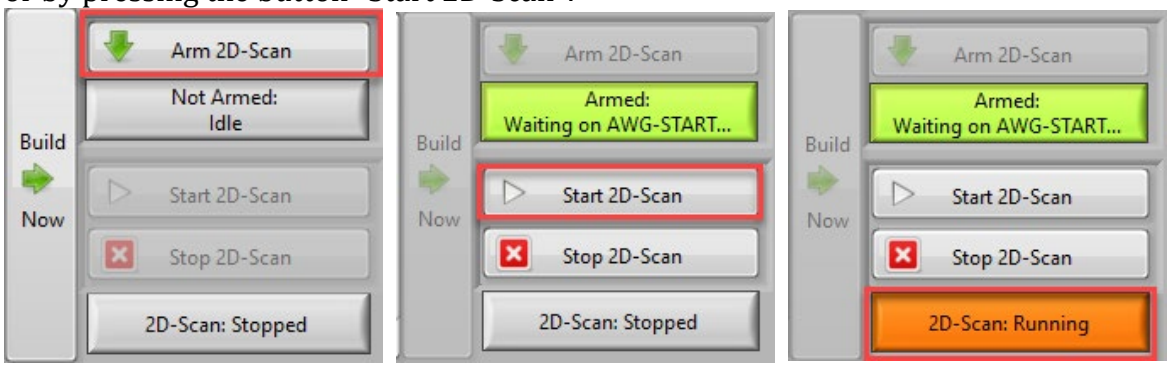
First, the 2D-Scan has to be built by pressing the "Build Now" button. Then INFORMATION and CAUTION message appears, since the selected DAC-Channels will be set to HBW and switched ON and the start voltages of the planned 2D-Scan will be applied:



After pressing "OK, go on!" the build process of the 2D-Scan will be started. This takes around seven seconds and then the button "Arm 2D-Scan" gets enabled.

Note: As soon as you make any change in the "Block 1: Setup 2D-Scan" the "Arm 2D-Scan" will be disabled and greyed out. Then you have to build the 2D-Scan again by pressing the "Build Now" button.

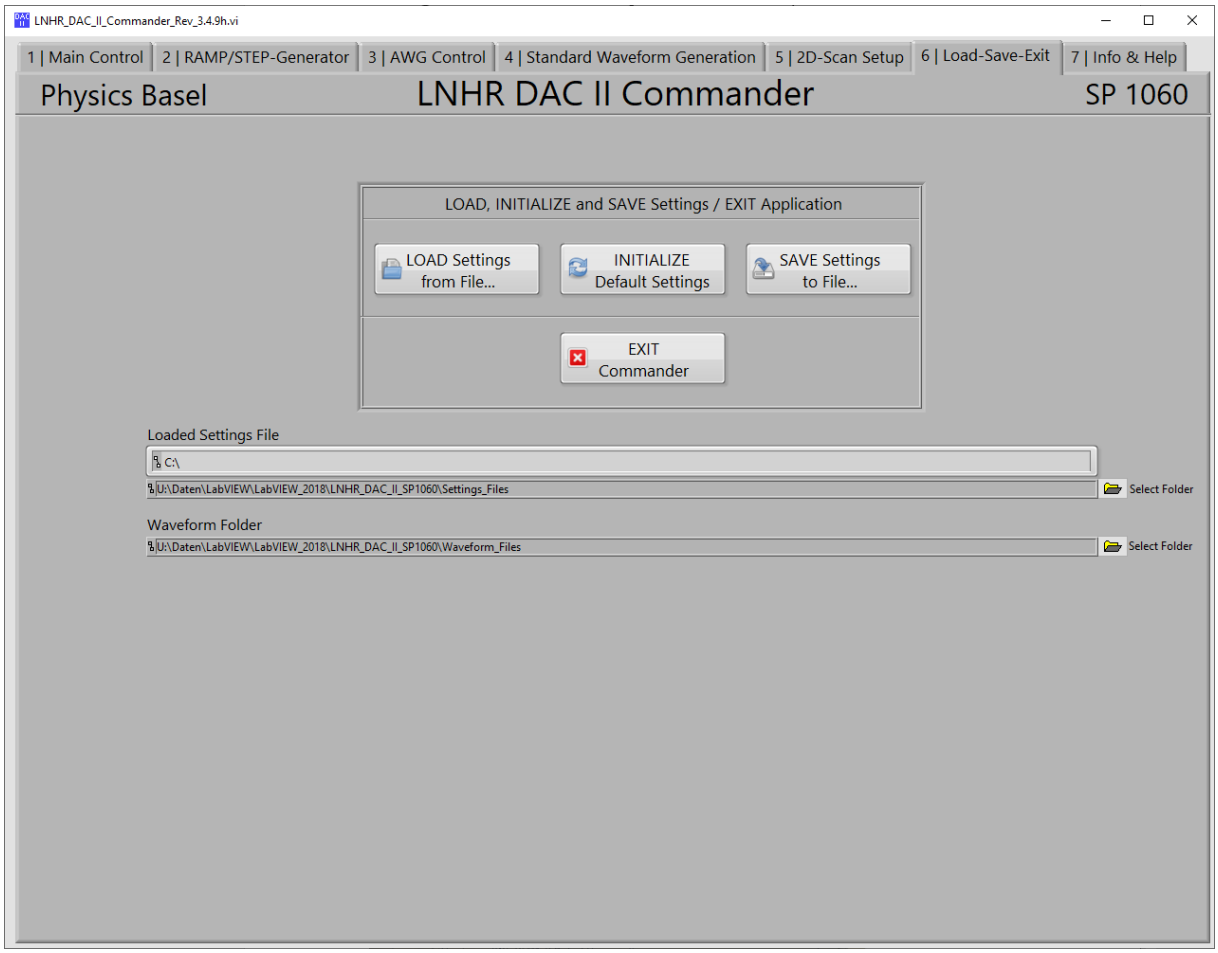
By pressing the button "Arm 2D-Scan" the x- and y-axis start voltages are set again and the external AWG-Trigger input is enabled – now the 2D-Scan is ready to be started. This can be done either by an external AWG-Trigger TTL-signal, by a remote-control command or by pressing the button "Start 2D-Scan":



A running 2D-Scan is indicated by changing its status from "2D-Scan: Stopped" to "2D-Scan: Running". Then the x/y-voltage graph in the "Block 2: Monitor 2D-Scan" are continuously updated with the actual x-voltage as a red line. A running 2D-Scan can be manually stopped (before it is finished) by pressing the "Stop 2D-Scan". The same 2D-Scan can be restarted by following the steps above beginning with "Arm 2D-Scan".

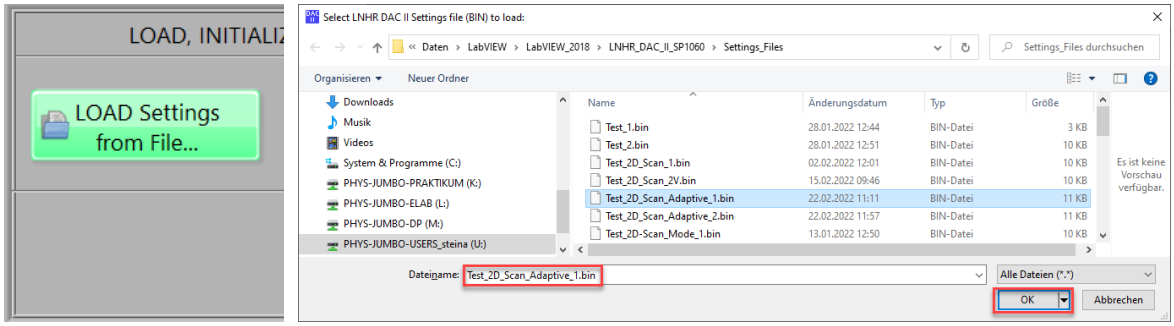
Note: Running more than two Adaptive 2D-Scans at the same time can overload the processor power of the LNHR DAC II. See the value "CPU-Load [%]" under "System-Health" in Tab 1. The "CPU-Load [%]" should always be smaller than 95%.

9 Tab 6 | Load-Save-Exit



On this Tab 6 “Load-Save-Exit” the settings of the LNHR DAC II Commander can be loaded, initialized to its default settings and saved to a file on the host PC. Further, the application can be exited and the location of the “Settings Folder” and the location of the “Waveform Folder” can be defined.

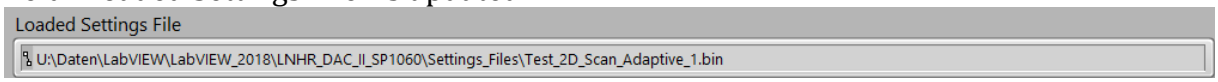
When pressing “LOAD Settings from File…” a system window with the title “Select LNHR DAC II Settings file (BIN) to load:” appears. Now, you can select the Settings file to be loaded:



Settings files are binary files and are not editable by the user. Only binary Settings files previously saved by the LNHR DAC II application can be loaded. Such a Settings file holds the values of all the controls of this application.
Bear in mind, when loading Settings files DAC-Channels may be automatically switched ON and set to an output voltage!

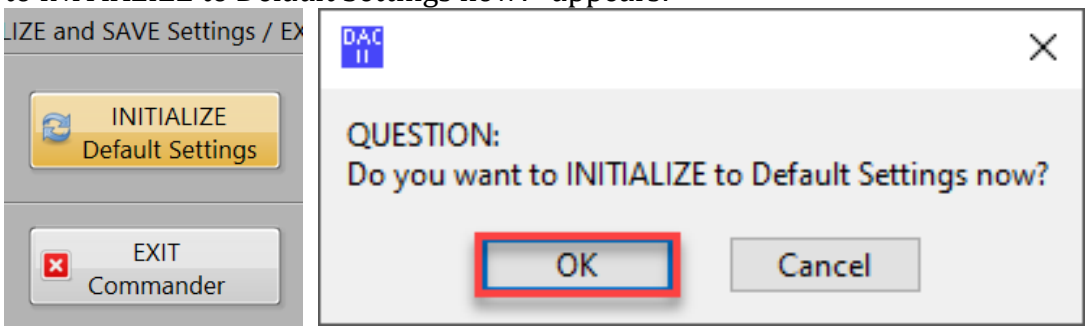
Note: The Wave-Memories are not loaded from these Settings files. The Wave-Memories must be separately loaded from text-files on Tab 4 – for description see chapter "Tab 4 | Standard Waveform Generation".

After selecting a binary file and pressing "OK" a short loading message is shown and the field "Loaded Settings File" is updated:



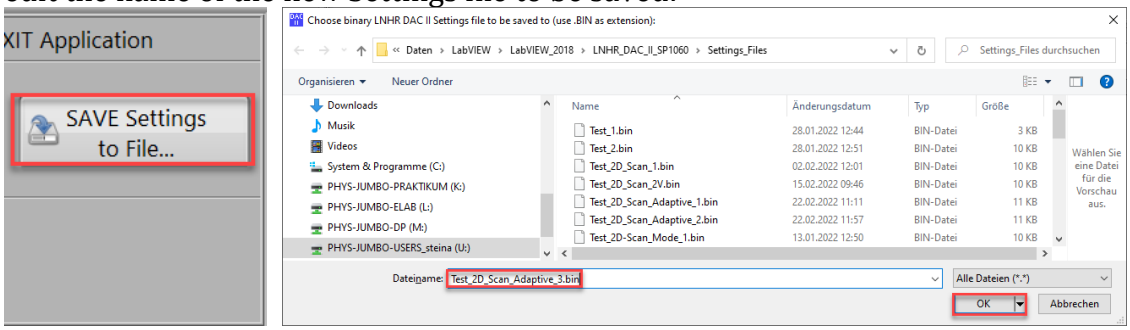
This field acts as a reminder for the actual loaded Settings and is valid until another Settings file is loaded or the application is initialized to its default settings – see below.

When pressing "INITIALIZE Default Settings" a window with the question "Do you want to INITIALIZE to Default Settings now?" appears:



Pressing "OK" will reset all controls to their initial values, as if you had restarted this application (e.g., all DAC-Channels OFF and on LWB) and the "Tab 1 | Main Control" is selected. The Wave-Memories are not affected by this initialization and are still hold their old values.

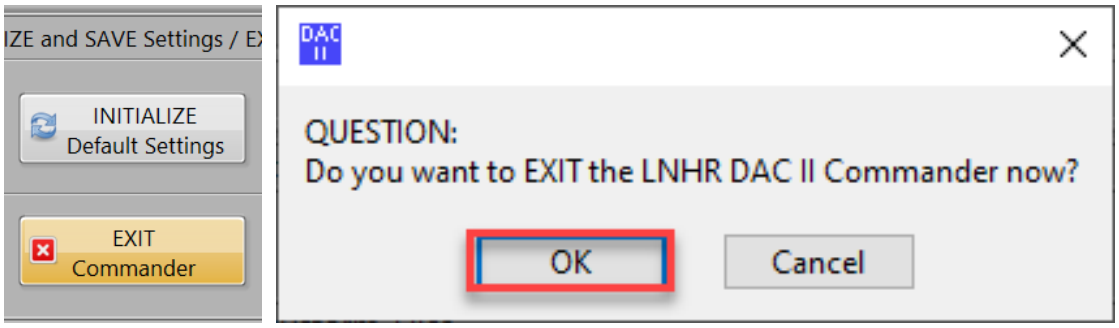
When pressing "SAVE Settings from File…" a system window with the title "Choose binary LNHR DAC II Settings file to be saved to (use .BIN as extension):" appears. Now, you can edit the name of the new Settings file to be saved:



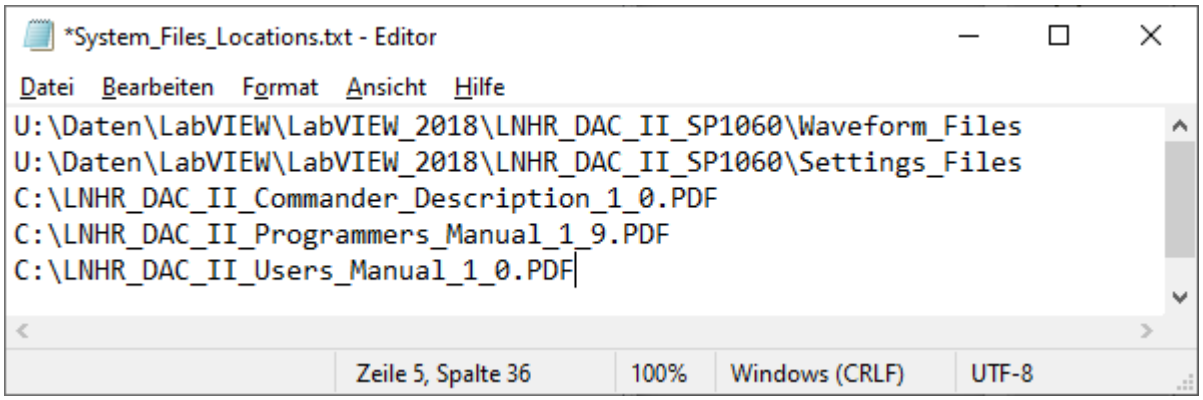
After pressing "OK" a short saving message is shown.

Note: The Wave-Memories are not saved to these Settings files. The Wave-Memories can be saved separately to text-files on Tab 4 – for description see chapter "Tab 4 | Standard Waveform Generation".

When pressing "EXIT Commander" a window with question "Do you want to EXIT the LNHR DAC II Commander now?" appears:

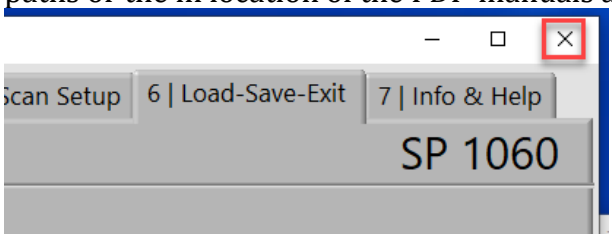


When pressing “OK” the application is closed and the file “System_Files_Locations.txt” is updated. This text file holds the paths for the “Waveform Files” and the “Settings Files” and the location of the PDF-manuals:



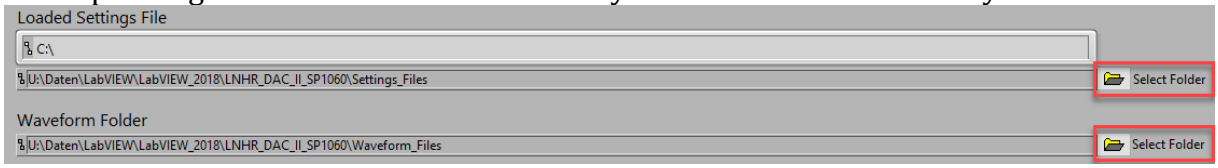
When the application is started the next time, these paths and locations are read. The user can also edit this file with a normal text editor.

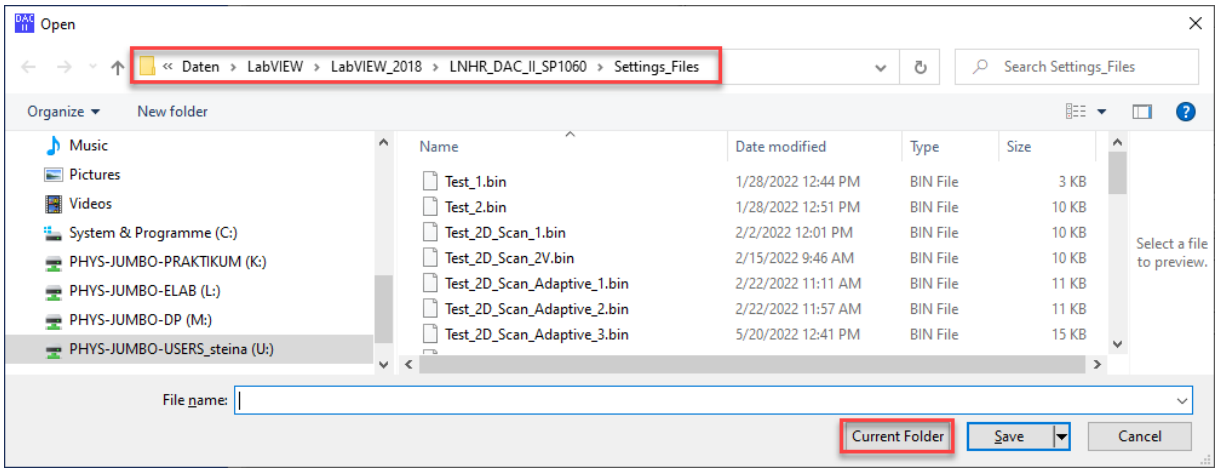
If you close the “LNHR DAC II Commander” application by using the normal close window button, the file “System_Files_Locations.txt” is not updated and any changes made in the paths or the in location of the PDF-manuals are lost:



Therefore, it is strongly recommended to use the “EXIT Commander” button to close the “LNHR DAC II Commander” application.

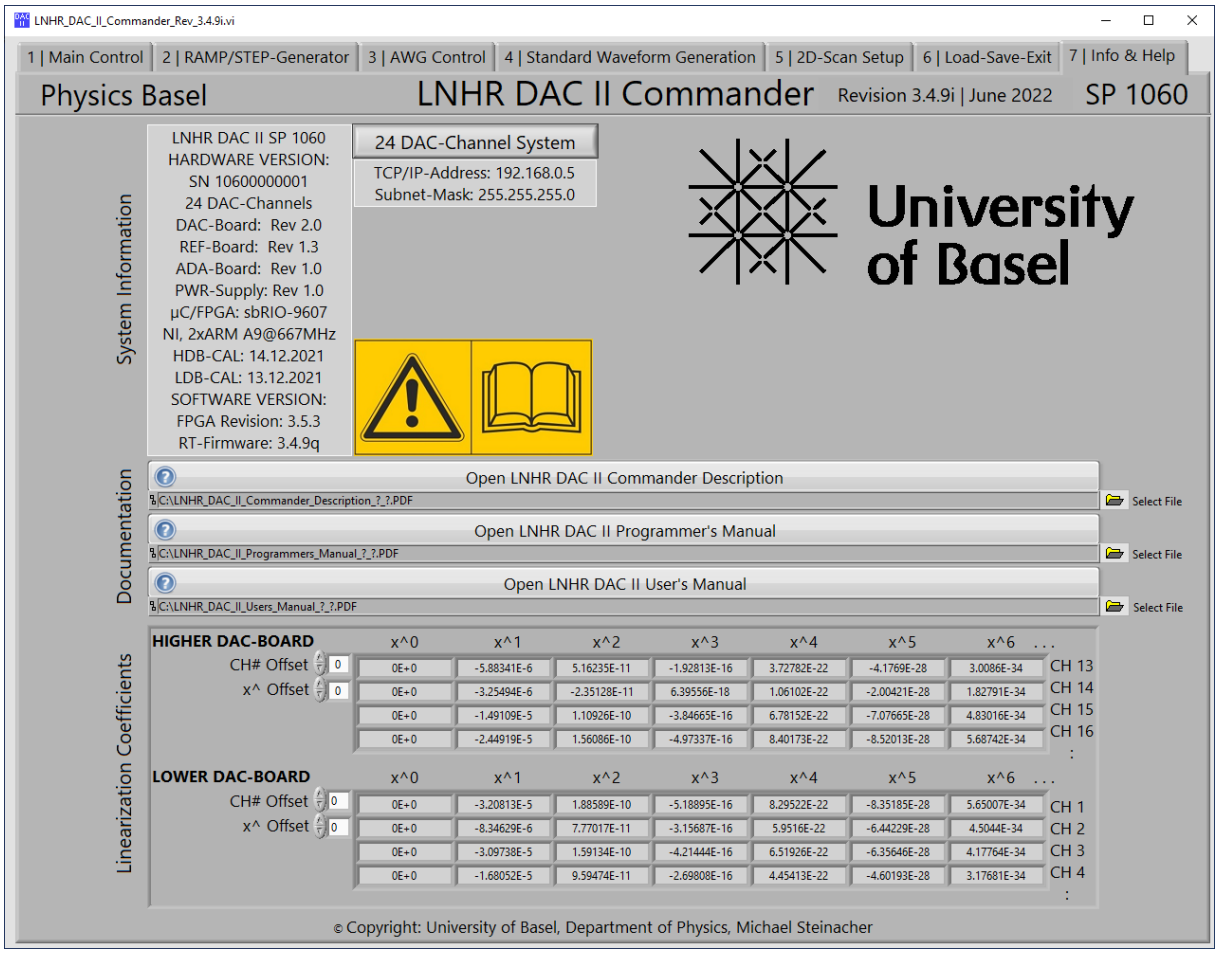
To select the locations of the “Settings Folder” and the “Waveform Folder” press the corresponding button “Select Folder” – then you can select the folder of your choice:





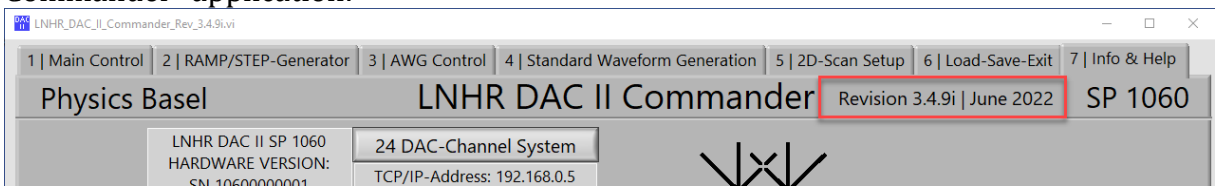
If you press “Current Folder” the path is used for loading the Settings or a Waveform. If you use the “EXIT Commander” button to close the “LNHR DAC II Commander” application, these paths are saved in the file “System_Files_Locations.txt” – see above.

10 Tab 7 | Info & Help

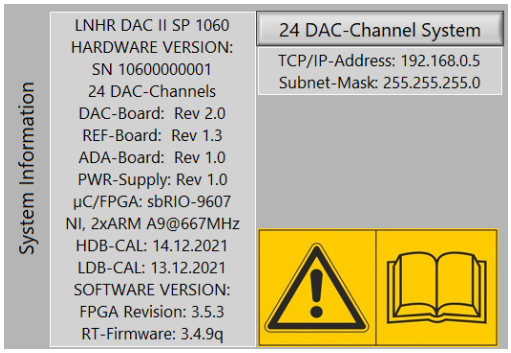


This Tab 7 “Info & Help” gives you the “System Information” on the LNHR DAC II. On this page also the fast access to the three PDF-manuals can be made and the “Linearization Coefficients” of both DAC-Boards are displayed.

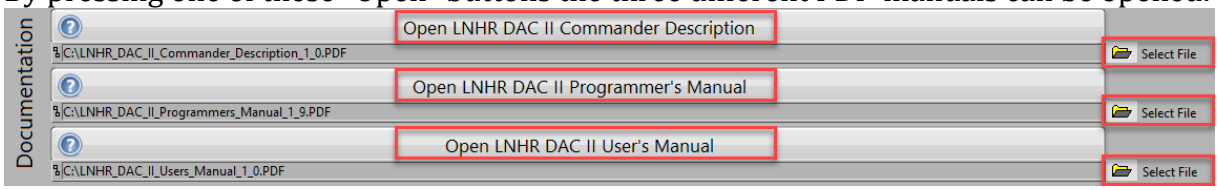
The top line of this Tab 7 shows the revision and the release date of this “LNHR DAC II Commander” application:



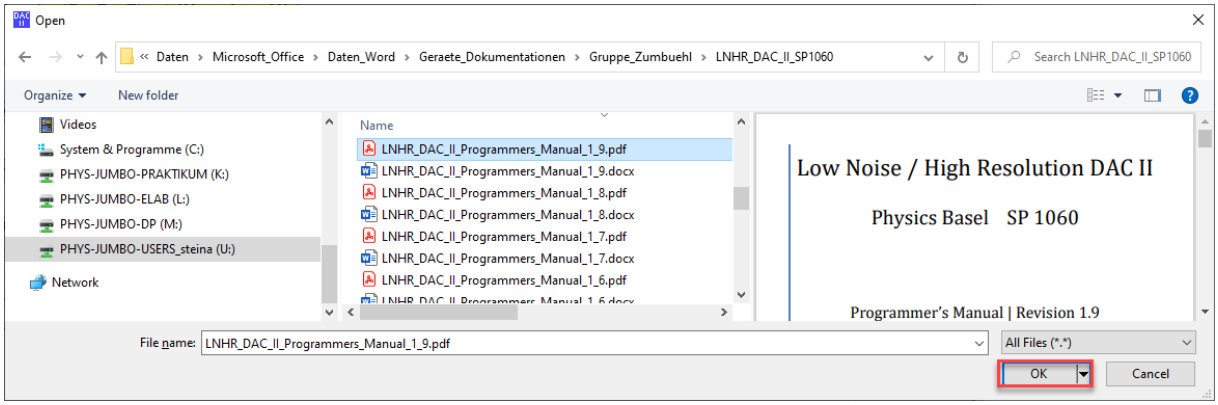
Here you can find the “System Information” on the LNHR DAC II hardware, the installed software and its network address:



By pressing one of these “Open” buttons the three different PDF-manuals can be opened:

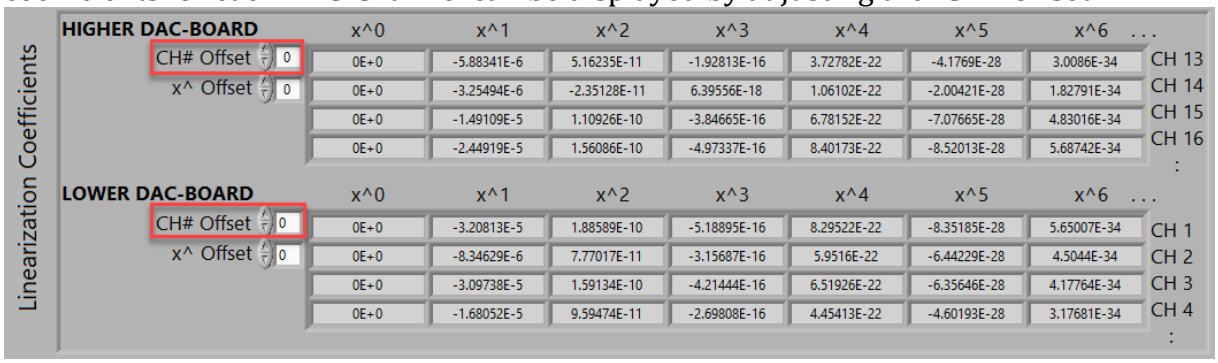


The locations of the PDF-manuals can be selected by using the three buttons “Select File”. Then



If you use the “EXIT Commander” button to close the “LNHR DAC II Commander” application, these locations of the PDF-manuals are automatically saved in the file “System_Files_Locations.txt” – see above.

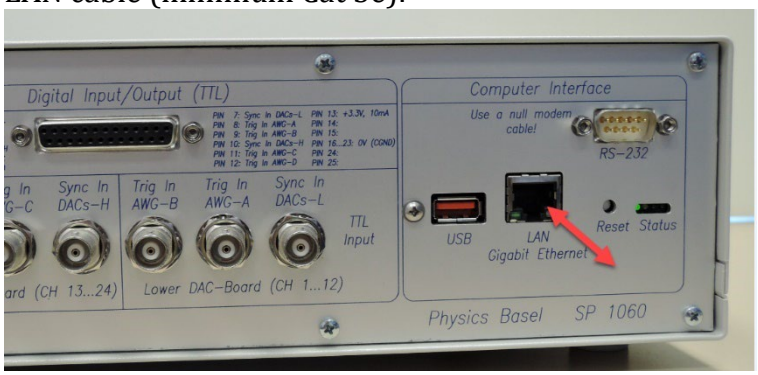
In the lower part the “Linearization Coefficients” of both DAC-Boards are shown – the coefficients for each DAC-Channel can be displayed by adjusting the “CH# Offset”:



This display is mainly used to check that the correct linearization coefficients have been saved on the LNHR DAC II and that they are read in correctly.

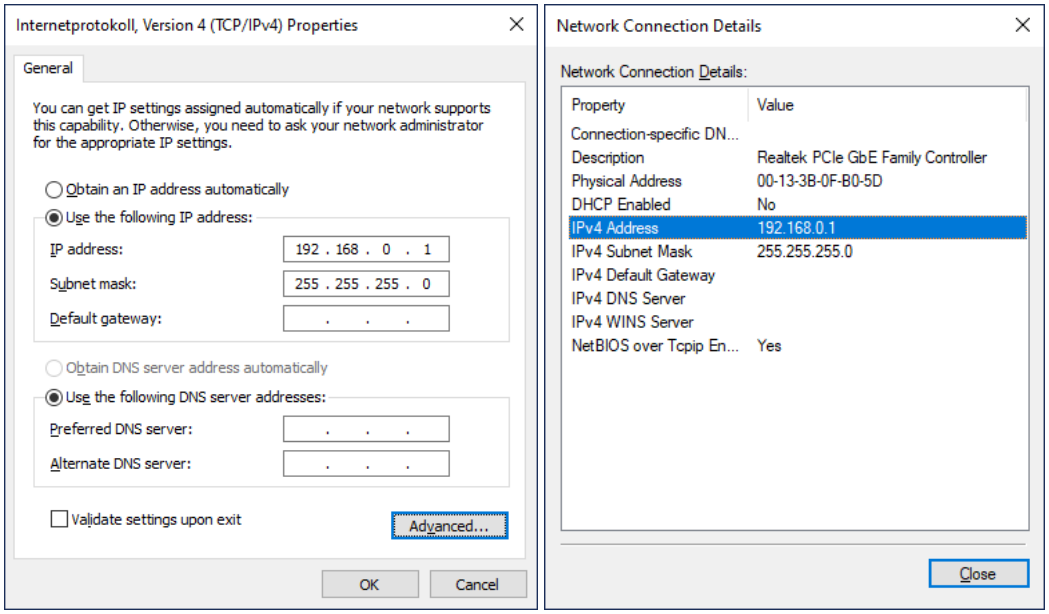
11 Network Connection

The private network interface card of host computer (Windows 10 PC) must be connected to the Gigabit Ethernet connector on the back of the LNHR DAC II by using a high-quality LAN cable (minimum Cat 5e):

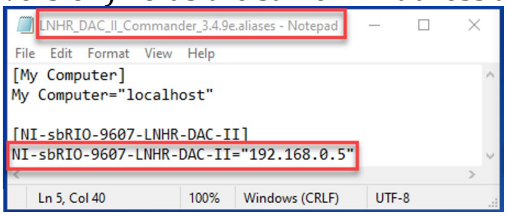


At delivery the TCP/IP-Address of the LNHR DAC II is set to 192.168.0.5 and the Subnet-Mask to 255.255.255.0, but it can be modified locally on the device under the menu item "TCP/IP Settings". Normally it is configured in a private network in the TCP/IPv4-address range from 192.168.0.0 to 192.168.255.255 (256 contiguous class C networks).

The data rate of 10 Mbps, 100 Mbps or 1 Gbps is automatically selected by the network interface card (NIC) of the host computer. The actual data rate is indicated by the right LED on the LAN port of LNHR DAC II: 10 Mbps=OFF, 100 Mbps=GREEN, 1 Gbps=YELLOW
The left LED on the LAN port shows the activity on the LAN; it is flashing when active.
Below the typical private network configuration of the NIC on the host computer is shown. The host IP-Address is set to 192.168.0.1 and its Subnet-Mask also to 255.255.255.0:

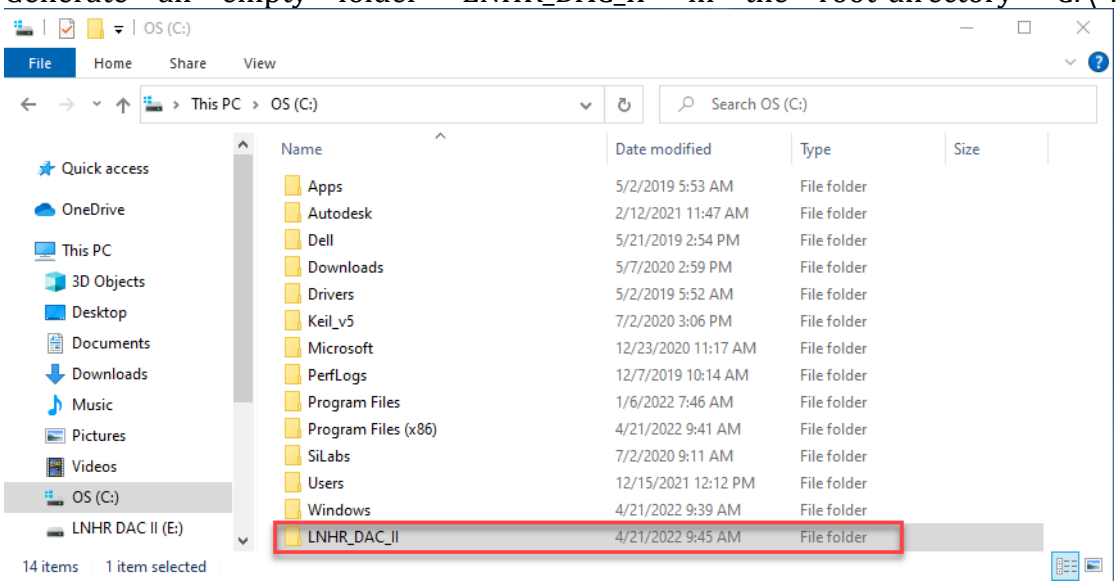


Make sure that the aliases-file "LNHR_DAC_II_Commander_3.4.9*.aliases" (* = build version) holds the same IP-Address as set on the "LNHR DAC II":



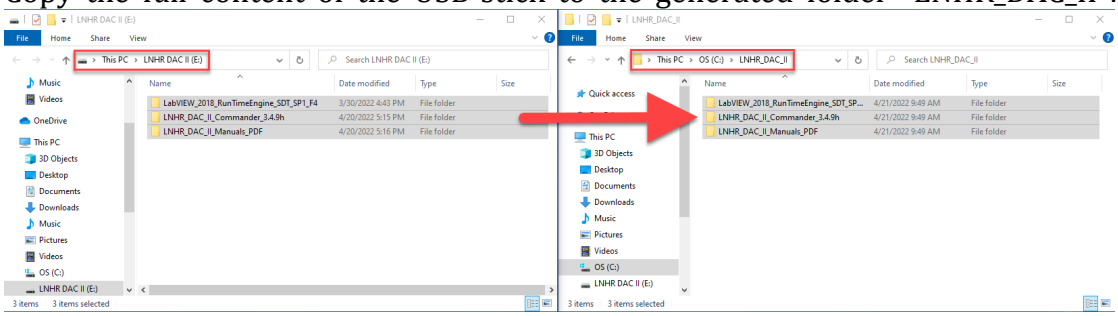
12 Installing the “LNHR DAC II Commander”

1. Generate an empty folder “LNHR_DAC_II” in the root-directory “C:\”:

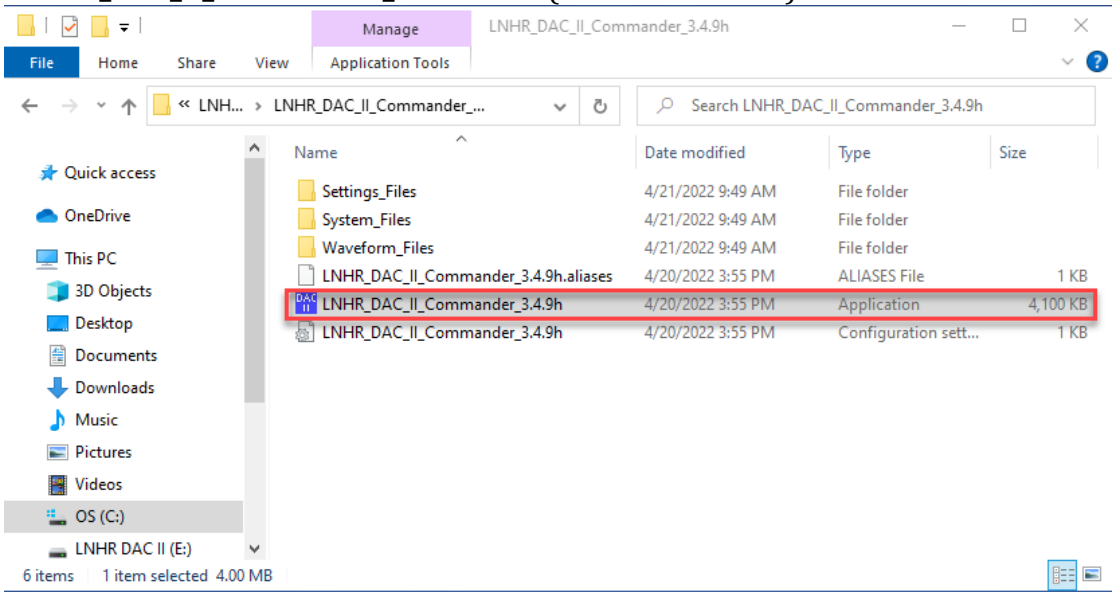


Of cause, you can also use a different location than the root-directory, but then you have to adapt the directory-names for the PDF-Manuals, the Settings-Files and the Waveform-Files.

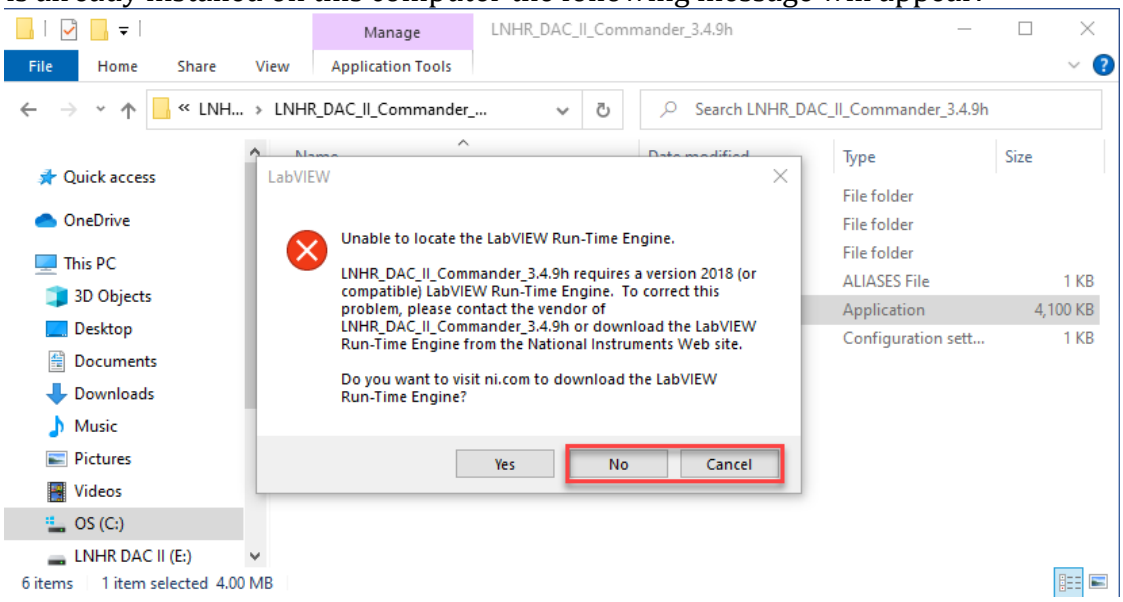
2. Copy the full content of the USB-stick to the generated folder “LNHR_DAC_II”:



3. Navigate to the subdirectory “C:\LNHR_DAC_II\LNHR_DAC_II_Commander_3.4.9*” (* = build version) and try to start the Commander Application “LNHR_DAC_II_Commander_3.4.9*.exe” (* = build version) with a double click:

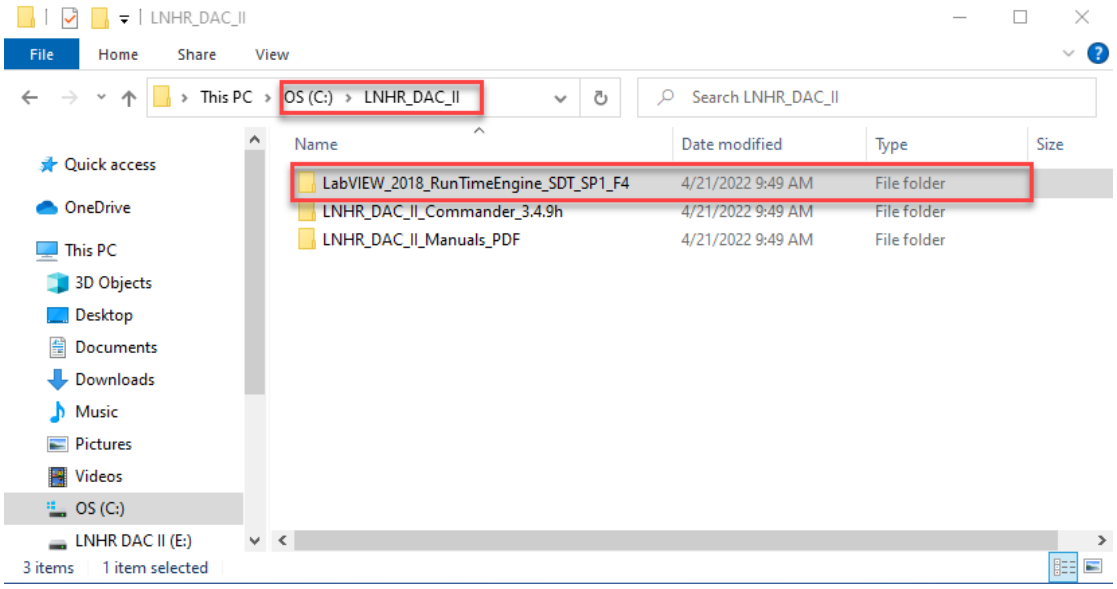


4. If no compatible LabVIEW Version (2018, SP1, Fix4) or LabVIEW Run-Time Engine is already installed on this computer the following message will appear:

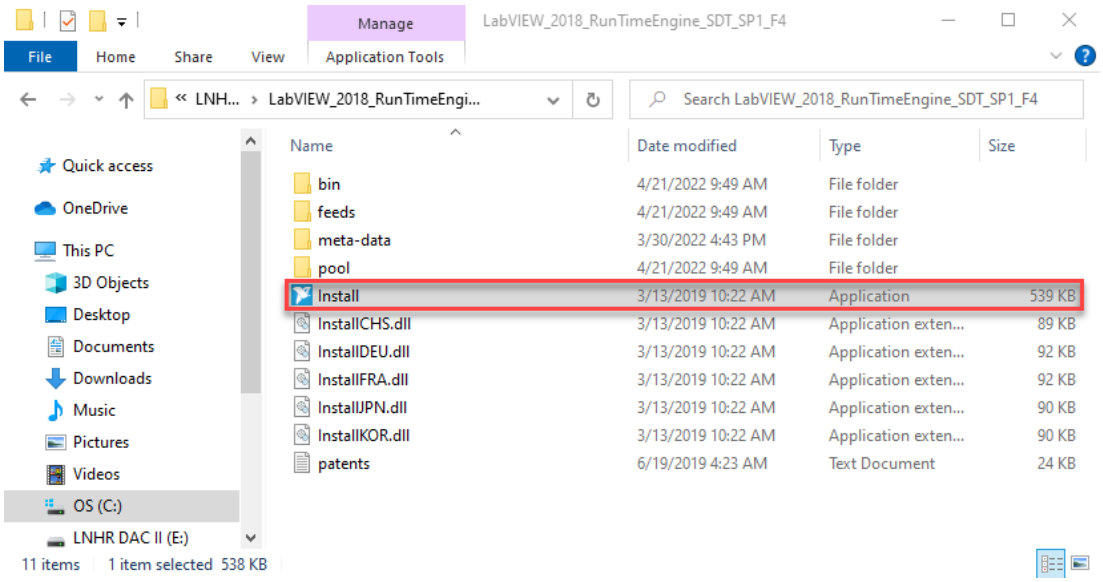


Note: Make sure that correct LabVIEW Run-Time Engine 2018, SP1, Fix4 is installed on the PC. Otherwise, the "LNHR DAC Commander" application may run, but not with optimal performance and with longer response time to user input!

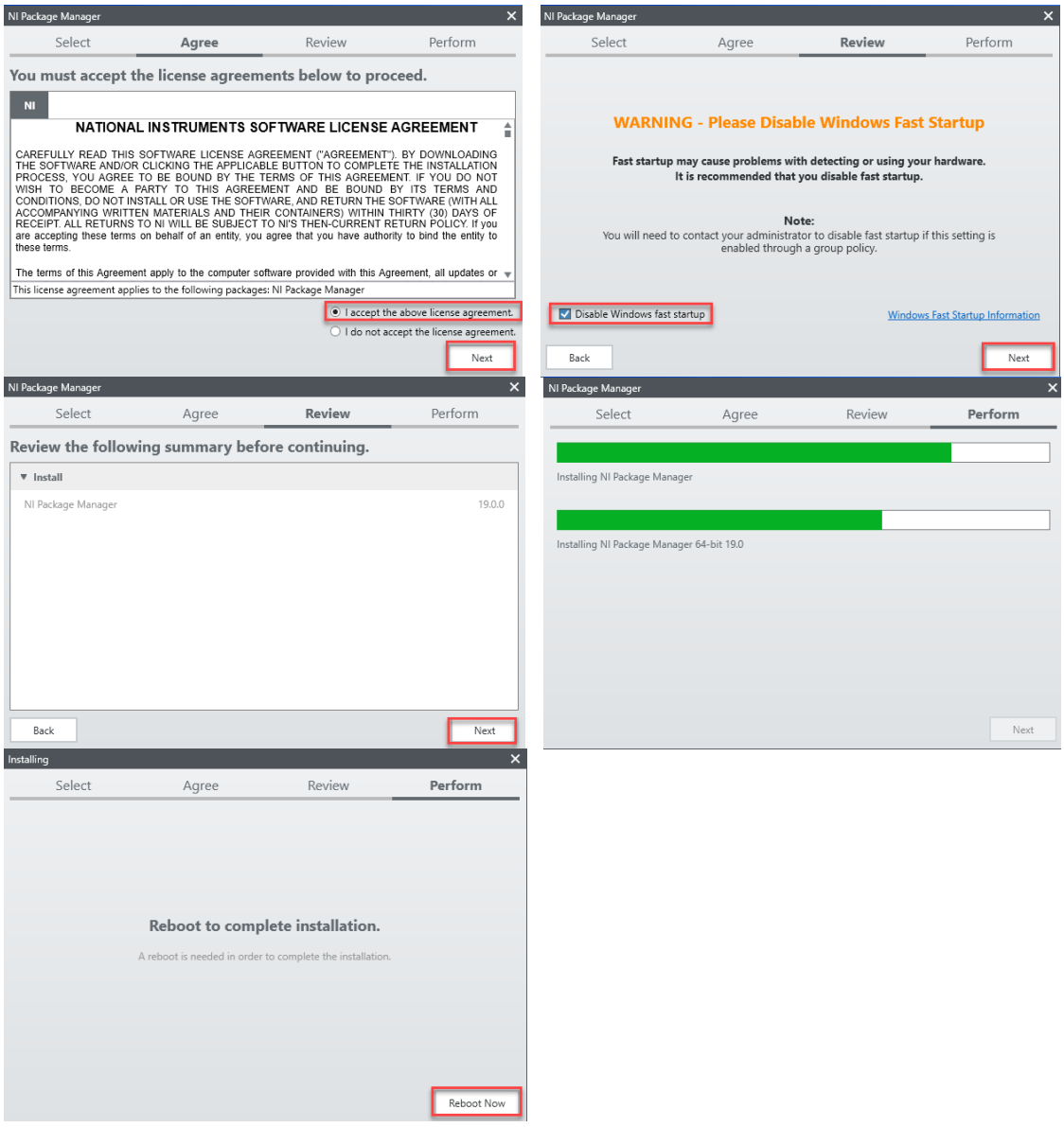
5. Select "No" or "Cancel" since the compatible LabVIEW Run-Time Engine exists already in the directory "LNHR_DAC_II". Open the folder "LabVIEW_2018_RunTimeEngine_SDT_SP1_F4" which holds the Run-Time Engine:



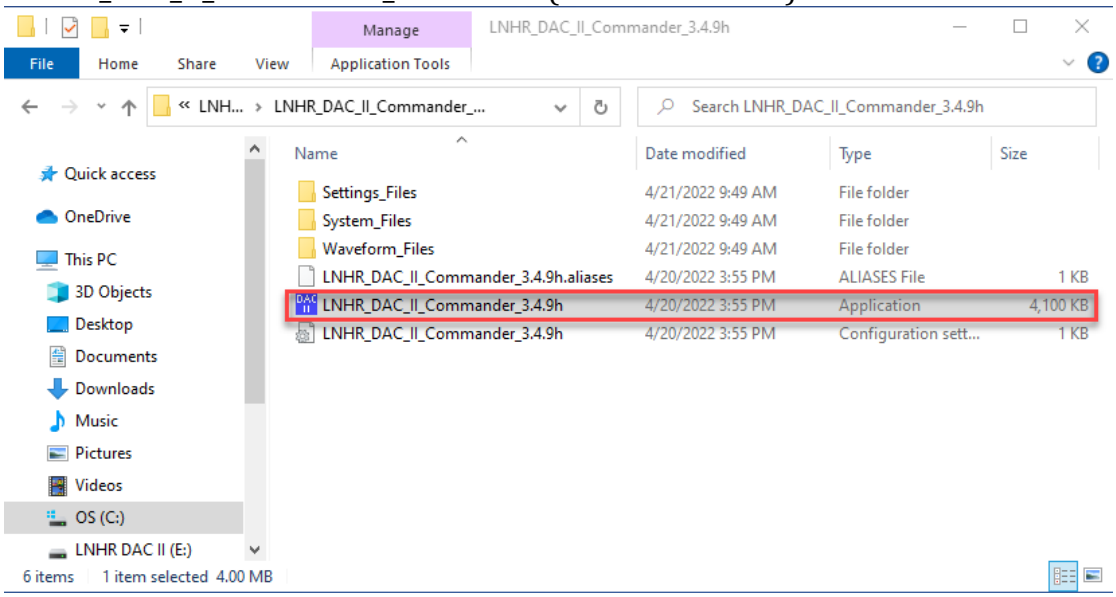
6. Select the "Install.exe" Application to start the installation of the appropriate LabVIEW Run-Time Engine (2018, SP1, Fix4):



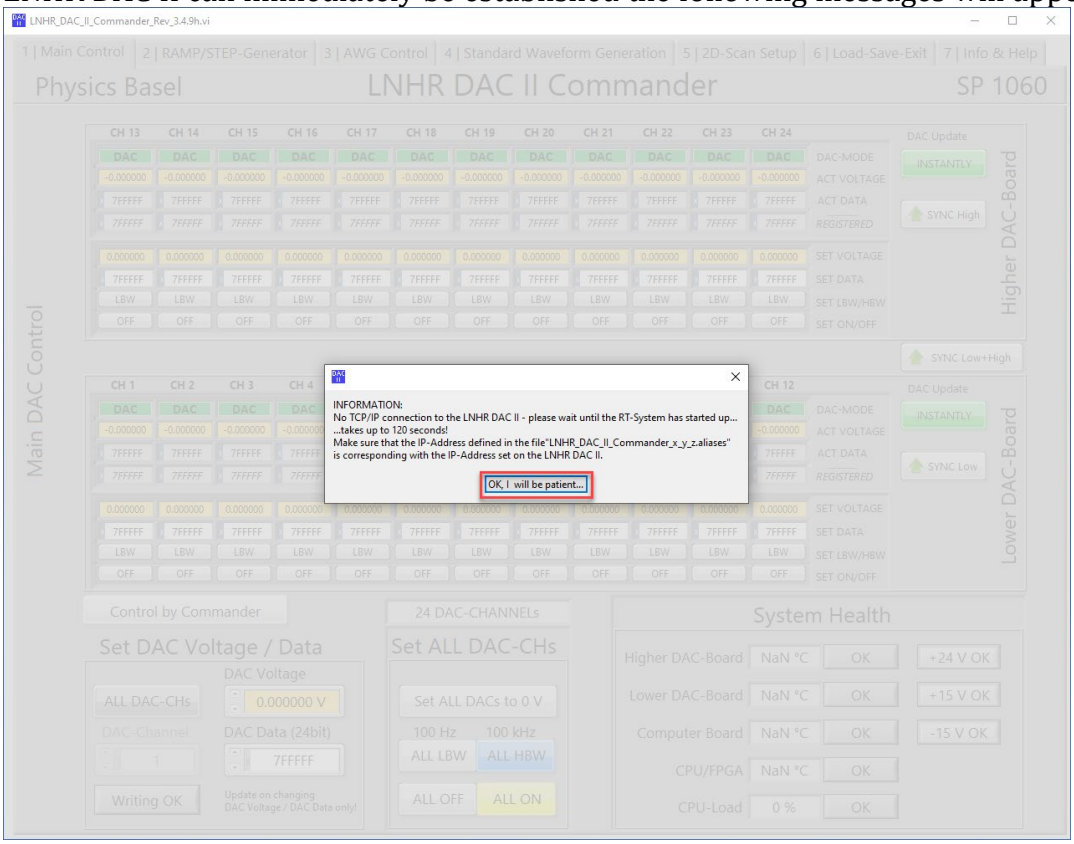
7. Follow the instructions to install the Run-Time Engine; at the end the PC has to rebooted:



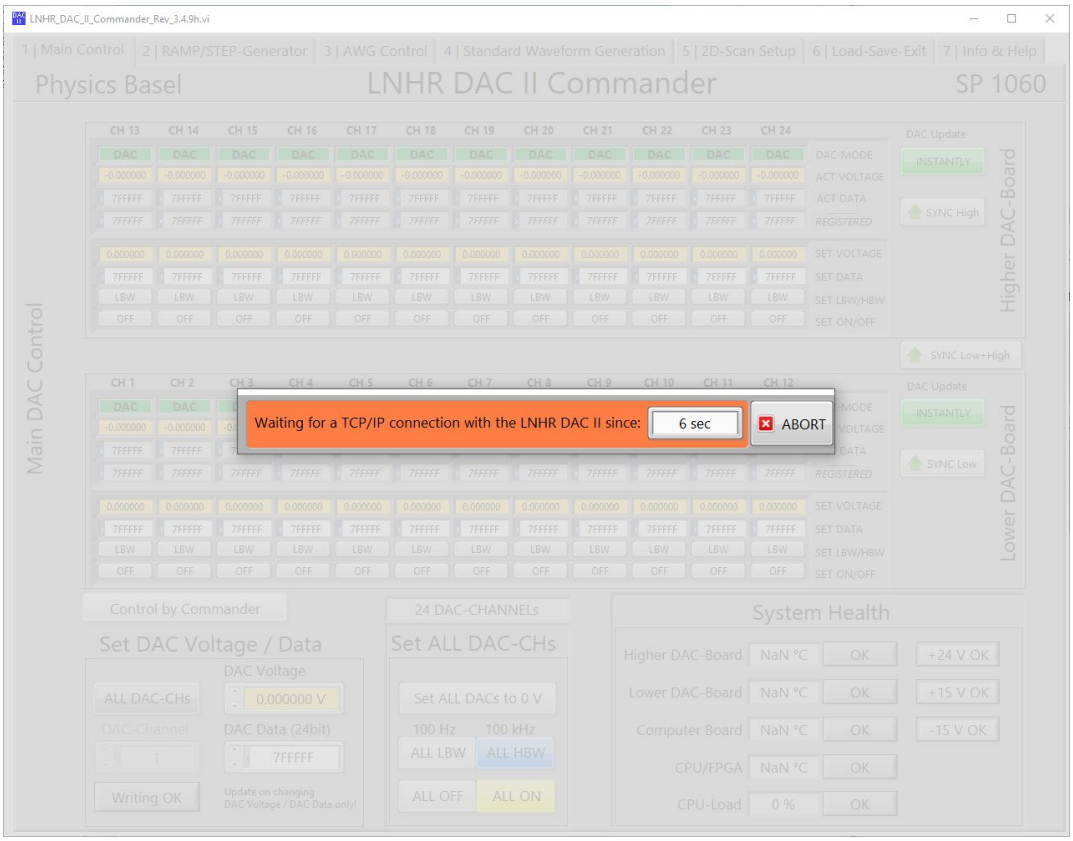
8. After the reboot of the PC try to start the Commander Application “LNHR_DAC_II_Commander_3.4.9*.exe” (* = build version) with a double click:



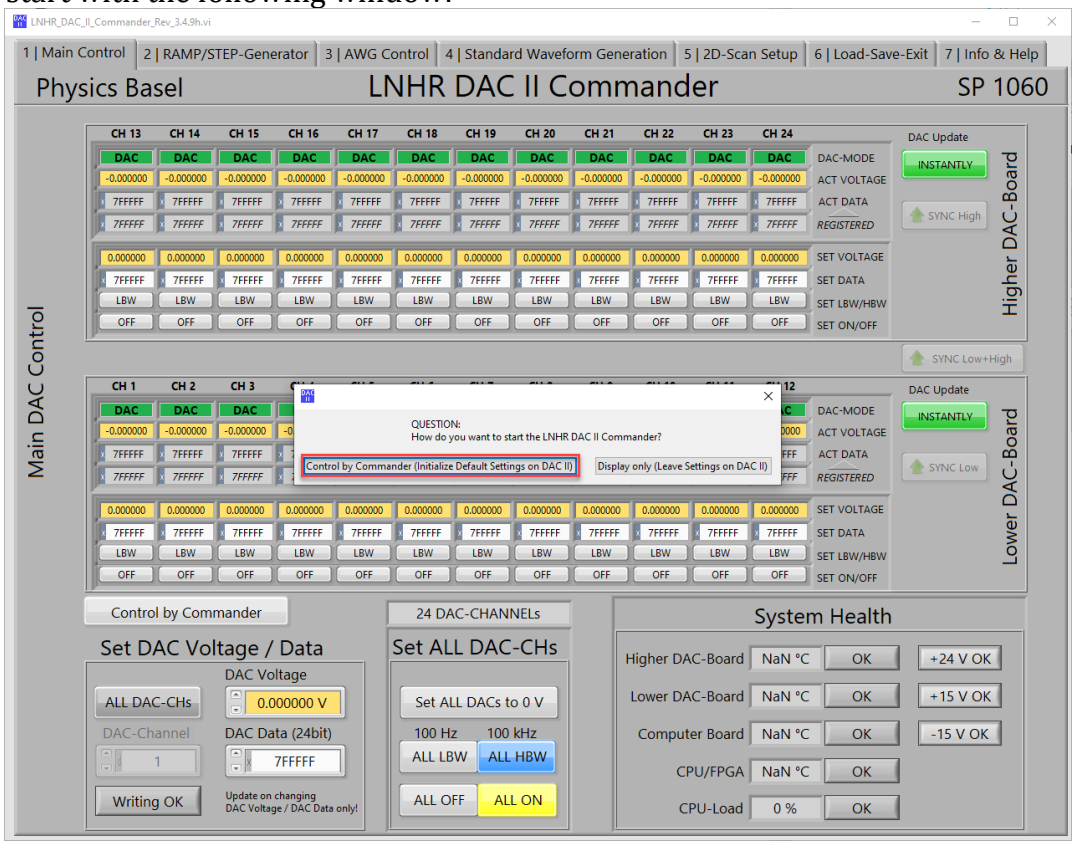
9. Now the Commander Application should start. If no network connection to the LNHR DAC II can immediately be established the following messages will appear:



When pressing “OK, I will be patient…” an orange window will appear and count down the seconds until the connection to the LNHR DAC II can be established:

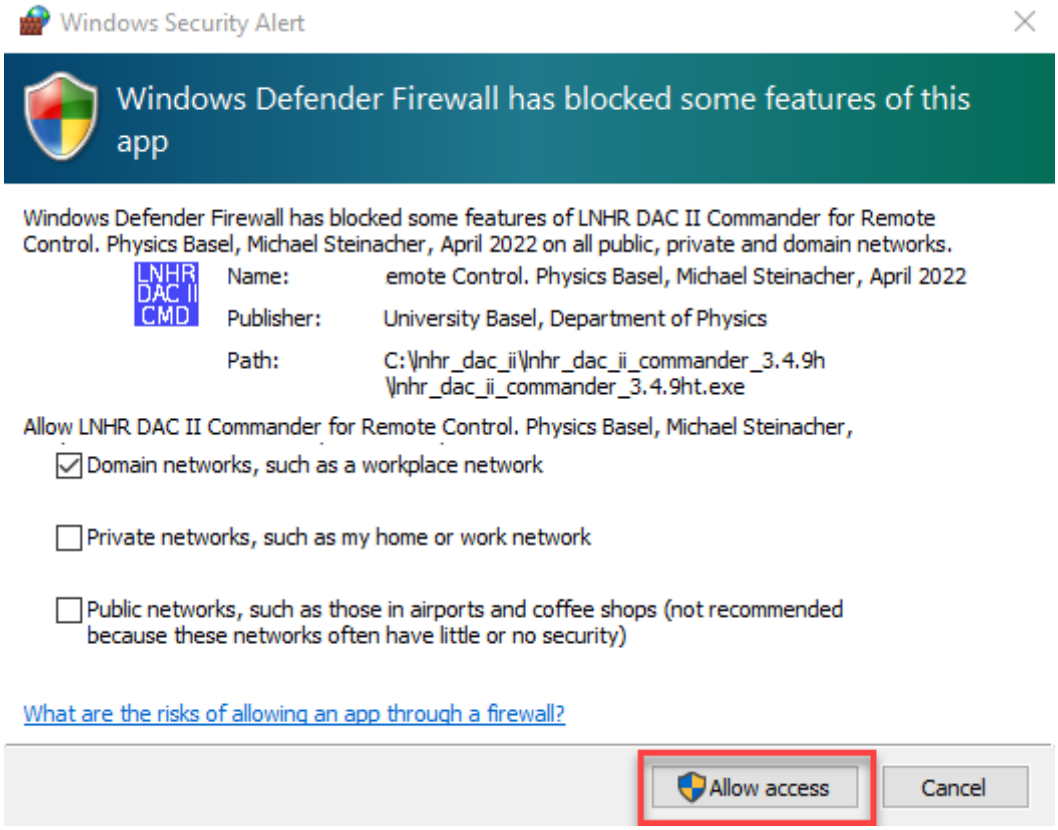


10. After maximum 120 seconds the LNHR DAC II Commander Application should start with the following window:



If no connection can be established, check the network settings on the device and on the network card on the Windows PC - see chapter "Network Connection".

11. Most probably, the Windows Defender Firewall will show this blocking message:



Select “Allow access” to make sure that the communication between the LNHR DAC and the PC isn’t blocked.

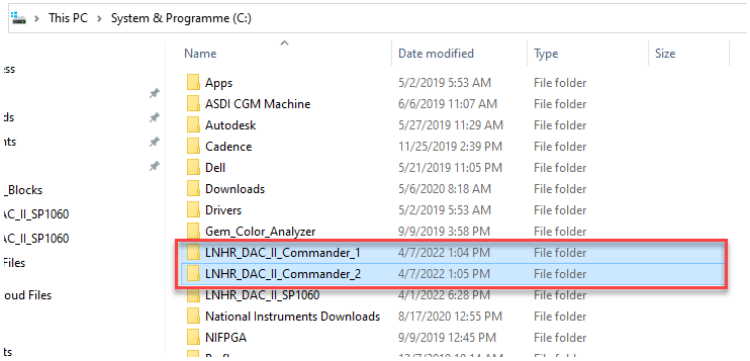
13 Controlling Multiple Devices

Multiple LNHR DACs II can be controlled by multiple Commanders running simultaneously in parallel. Doing so, each device has its own Commander-Window for display and controlling. The Ethernet cables of all the devices have to be connected to the host computer by using a multiport switch. Theoretically, up to 253 devices could be controlled by assigning different IP-Addresses.

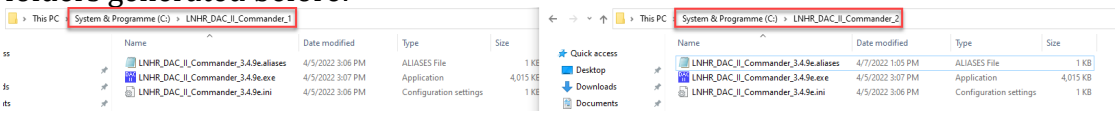
If more than one LNHR DAC II has to be controlled, the following steps must be taken (this example shows how to control two devices):

1. Assign different IP -Addresses to the two devices. This has to be done locally by using the LCD and the encoder/pus-button under the menu item “TCP/IP Settings”. In the example below the lower LNHR DAC II (SN 1060000001) has an IP-Address of 192.168.0.5 while the upper device (SN 1060000002) is set to 192.168.0.6:

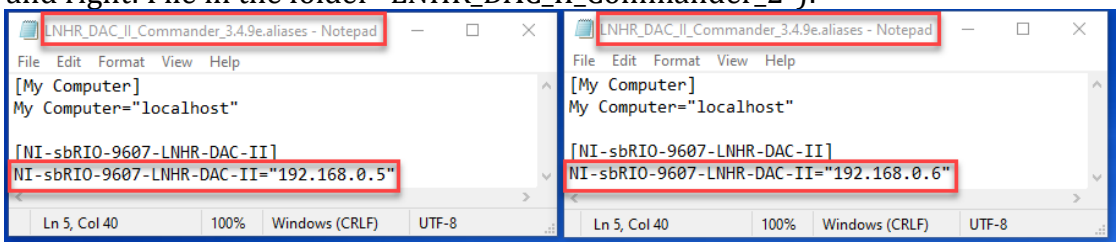
2. Generate two empty folders in the directory where your programs are normally located. In this example the two folders are named “LNHR_DAC_II_Commander_1” and “LNHR_DAC_II_Commander_2” and they are generated in the root-directory “C:\”:



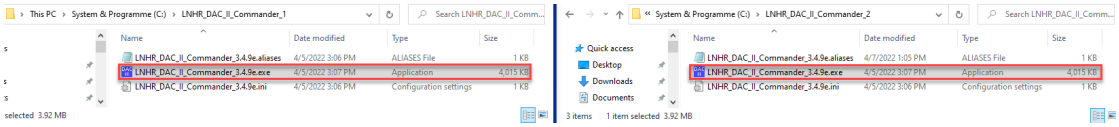
3. From the on the USB-stick copy the content (three files) in the subdirectory "LNHR_DAC_II_Commander_3.4.9*" (* = build version) into the two different folders generated before:



4. Modify the two text-files "LNHR_DAC_II_Commander_3.4.9*.aliases" so that the IP-Addresses given on the line "NI-sbRIO-9607-LNHR-DAC-II=" fits to the corresponding device address: 192.168.0.5 for the DAC number 1 and 192.168.0.6 for the DAC number 2. This modification can be done by using the Notepad Editor. Do not forget to save your changes with "File…Save". The two aliases-files in the two folders looks like this (left: File in the folder "LNHR_DAC_II_Commander_1" and right: File in the folder "LNHR_DAC_II_Commander_2"):

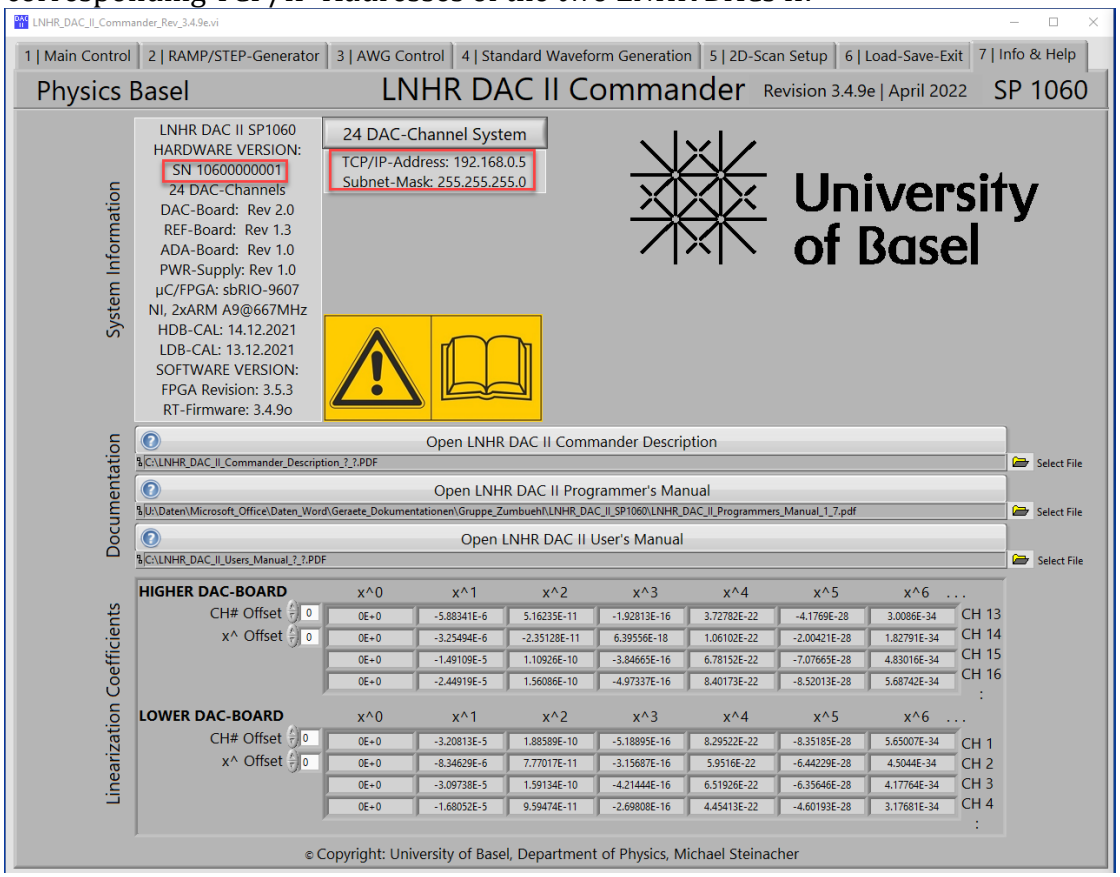


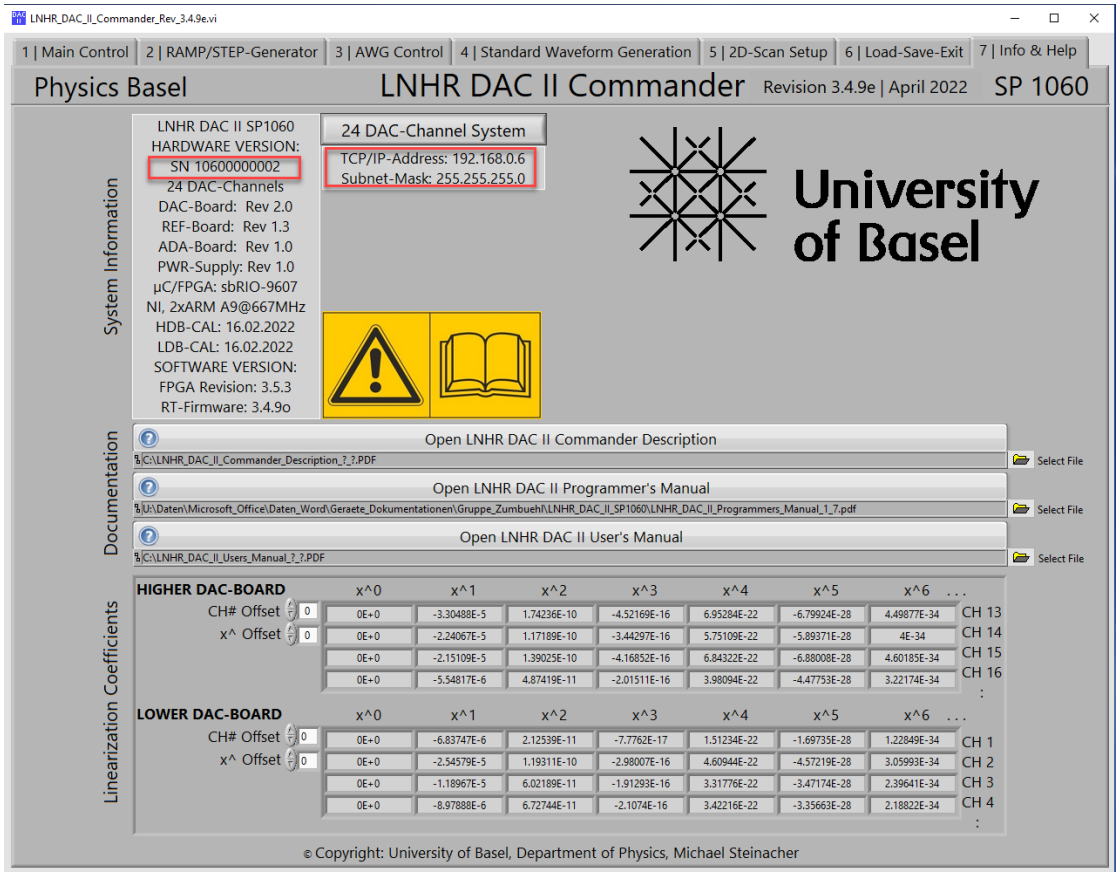
5. Now, the two Commander-Applications "LNHR_DAC_II_Commander_3.4.9*.exe" can be started from the two different folders:



6. Since the two aliases-files hold two different IP-Addresses the two Commander-Applications will connect automatically to the corresponding LNHR DAC II with the corresponding IP-Address. The two windows of the two LNHR DAC II Commanders give now fully access to the 48 DAC-Channels:

7. In the two Tabs "Info & Help" you can find the serial numbers and the corresponding TCP/IP-Addresses of the two LNHR DACs II:





14 Converting DAC-Voltage to DAC-Value

A DAC-Value is a 24-bit number in the decimal range from 0 to 16'777'215 (2^{24}-1); this corresponds to a hexadecimal range from 0x000000 to 0xFFFFFF.

The DAC-Voltage has a fixed range from -10 V to +10 V with a step-size of 1.192093 µV (20 V / 16'777'215).

For a given DAC output voltage (Vout [-10 V ...+10 V]) the 24-bit decimal DAC-Value (DACval [0…16'777'215]=[0x000000…0xFFFFFF]) is given by (rounded to the next integer value):

$$DACval\_dec = (Vout + 10) \cdot 838'860.74$$

To get a DAC-Value (HEX), which is needed for remote programming the DAC output voltage, the decimal number has to be converted to a hexadecimal number. All higher program languages have already included such a conversion-function.

For a given decimal DAC-Value (DACval_dec [0...16'777'215]=[0x000000…0xFFFFFF]) the DAC output voltage (Vout [-10 V...+10 V]) can be determined by:

$$Vout = (DACval\_dec / 838'860.74) - 10$$

The table below shows the DAC-Voltage [±10 V] in 1 V steps and the calculated DAC-Value (decimal) and the corresponding DAC-Value (HEX):

DAC-Voltage	DAC-Value (decimal)	DAC-Value (HEX)
+10 V	16'777'215	0xFFFFFF
+9 V	15'938'354	0xF33332
+8 V	15'099'493	0xE66665
+7 V	14'260'633	0xD99999
+6 V	13'421'772	0xCCCCCC
+5 V	12'582'911	0xBFFFFF
+4 V	11'744'050	0xB33332
+3 V	10'905'190	0xA66666
+2 V	10'066'329	0x999999
+1 V	9'227'468	0x8CCCCC
0 V	8'388'607	0x7FFFFF
-1 V	7'549'747	0x733333
-2 V	6'710'886	0x666666
-3 V	5'872'025	0x599999
-4 V	5'033'164	0x4CCCCC
-5 V	4'194'304	0x400000
-6 V	3'355'443	0x333333
-7 V	2'516'582	0x266666
-8 V	1'677'721	0x199999
-9 V	838'861	0x0CCCCD
-10 V	0	0x000000

15 Table of Content