Low Noise / High Resolution DAC II

Physics Basel SP 1060

User's Manual | Revision 1.2a

For Software Release 3.4.9

Michael Steinacher | November 2022

University of Basel

1 Key Features

- 24 (12) DAC-Channels with a voltage range of ±10 V
- 24-bit resolution (1.2 µV step size), independent of the selected bandwidth
- Selectable bandwidth between 100 Hz (LBW) or 100 kHz (HBW)
- Low noise performance:
  LBW @V_{DAC} = 0 V (0.1 Hz…100 Hz): 300 nV_{RMS}
  LBW @V_{DAC} = ±10 V (0.1 Hz…100 Hz): 500 nV_{RMS}
  HBW @V_{DAC} = 0V… ±10 V (0.1 Hz…100 kHz): 4 μV_{RMS}
- Low temperature drift: 1 µV/K + 1.5 ppm/K (from actual DAC voltage)
- Low Nonlinearity (INL): ±7 LSB
- Selectable DAC-Channel ON/OFF (OFF: Grounded via 1 Mega Ohm)
- 50 Ohm output impedance in ON state
- 1 mA output current on all DAC-Channels and 10 mA on one DAC-Channel per board
- DAC outputs can be synchronously updated (external or via command)
- Four independent RAMP/STEP-Generators
- Four (two @12 DACs) AWG-Channels with waveform generation options
- Independent DAC channels with a crosstalk isolation of >137 dB
- Output ground is isolated from housing and computer interface
- LC-Display for status/voltage display and local manual control
- Remote controllable via Ethernet (TCP/IP Telnet) or RS-232
- AWG and STEP-Generator can be combined for a fast two-dimensional Scan (2D-Scan); up to four (two @12 DACs) parallel running 2D-Scans
- User friendly Windows application “LNHR DAC II Commander” allows to control the device and simply setup 2D-Scans (also adaptive 2D-Scans)
- LabVIEW 2018 drivers and sample programs are included (for TCP/IP Telnet and RS-232 remote control)
- Single 24 V Power supply (wall plug power supply included)
- Compact and robust 19” desktop and rack mount housing (2U Height)

2 Safety Precautions 

- The Low Noise / High Resolution DAC II (LNHR DAC II) is designed for indoors dry laboratory use by qualified and authorized persons only.
- Read this manual carefully before installing and use the LNHR DAC II; all the safety precautions must be respected.
- Do not remove any cover. Since the internal parts are precisely adjusted, do not try to adjust or modify any part of the LNHR DAC II.
- Make sure that the housing of the device is always connected to ground/earth; when not mounted in a grounded 19” rack, use the ground socket on the back panel.
- The external bias voltage must not exceed ±20 V with respect to ground/earth; it is internally restricted to ±25 V by Zener-Diodes.
- This device is not approved for use on humans or animals.

3 Disclaimer

Physics Basel hereby disclaims all responsibility for personal injury, property damage and fine of penalty which results from misuse, not respecting the safety precautions, improper maintenance or improper application of this product.
Compliance with all applicable environment and personnel safety regulations is the sole responsibility of the user.

4 Used Abbreviations

The Following abbreviations are used in this manual:
LNHR = Low Noise / High Resolution
DAC = Digital/Analog Converter
LED = Light Emitting Diode
LCD = Liquid Crystal Display
CPU = Central Processing Unit
FPGA = Field Programmable Gate Array
BNC = Bayonet Nut Connector
TTL = Transistor-Transistor Logic
AWG = Arbitrary Waveform Generator
WAV = Wave
RMP = Ramp
LBW = Low Bandwidth (100 Hz)
HBW = High Bandwidth (100 kHz)
SWG = Standard Waveform Generation
POLY = Polynomial
2D = Two-Dimensional
HEX = Hexadecimal
msec = milli-second (1E-3)
µsec = micro-second (1E-6)
ppm = Parts per million (1E-6)
AGND = Analog Ground
INL = Integral Nonlinearity
FFT = Fast Fourier Transformation
RMS = Root Mean Square (Effective Value)

5 Overview

This documentation applies to the LNHR DAC II (SP 1060) with 24 DAC-Channels and with a Software Release of 3.4.9 - you can easily check the installed release on the local LCD under the menu item “Software Release”.

Two different version of the LNHR DAC II are available:
The fully equipped 24 DAC-Channels version and the 12 DAC-Channels version which has only one DAC-Board (Lower DAC-Board) with the DAC-Channels 1 to 12. Since all other components are the same (including the front-panel) the 12 DAC-Channels version can later be upgraded to a 24 DAC-Channels version; for this upgrade the device has to be returned to the manufacturer (Physics Basel).

This “User’s Manual” documents the fully equipped 24 DAC-Channels version. For the 12 DAC-Channels version some options and numbers are different than indicated in this manual, since the Higher DAC-Board with the DAC-Channels 13 to 24 are missing.

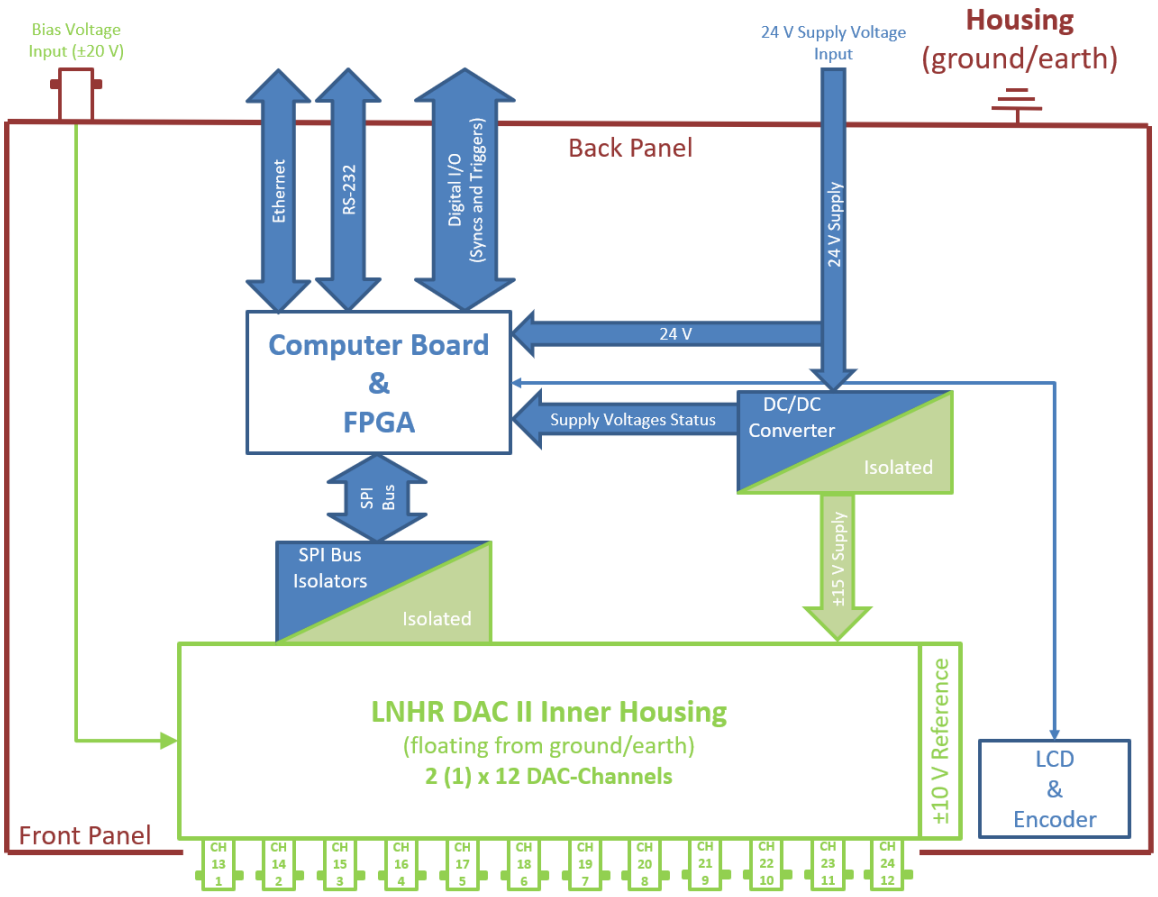
For further information see also the “LNHR DAC II Programmer’s Manual” and the “LNHR DAC II Commander Description” – the Commander is a Windows application to control and setup the device.

6 Description and Applications

The LNHR DAC II generates 24 independent, low noise and ultra-stable voltages. To reach the optimal stability the device has to be warmed-up for at least two hours. The output range of ±10 V, combined with the 24-bit resolution, allows adjusting the voltages with a step size of only 1.2 µV.

Such low noise and ultra-fine tunable voltages are often needed in fundamental physics experiments at very low-temperatures. The samples in the cryostat are cooled near to absolute zero Kelvin. For such experiments, constant DC bias-voltages and ramp-voltages with low noise performance are mandatory to drive the gate voltages of the very cold sample. Since the typical load resistance of such gates is very high (>100 Mega Ohm), the 50 Ohm output source impedance of the LNHR DAC II can be neglected.

To ensure that the DAC voltages are perfectly referenced to the cryostat ground, no ground loop currents must flow between the cryostat and the LNHR DAC II. This is achieved by installing the DAC-Channels in galvanically isolated "Inner Housing", which can be floating by maximum ±20 V with respect to the outer housing which is on grounded/earth. The block diagram of the LNHR DAC II is given below:



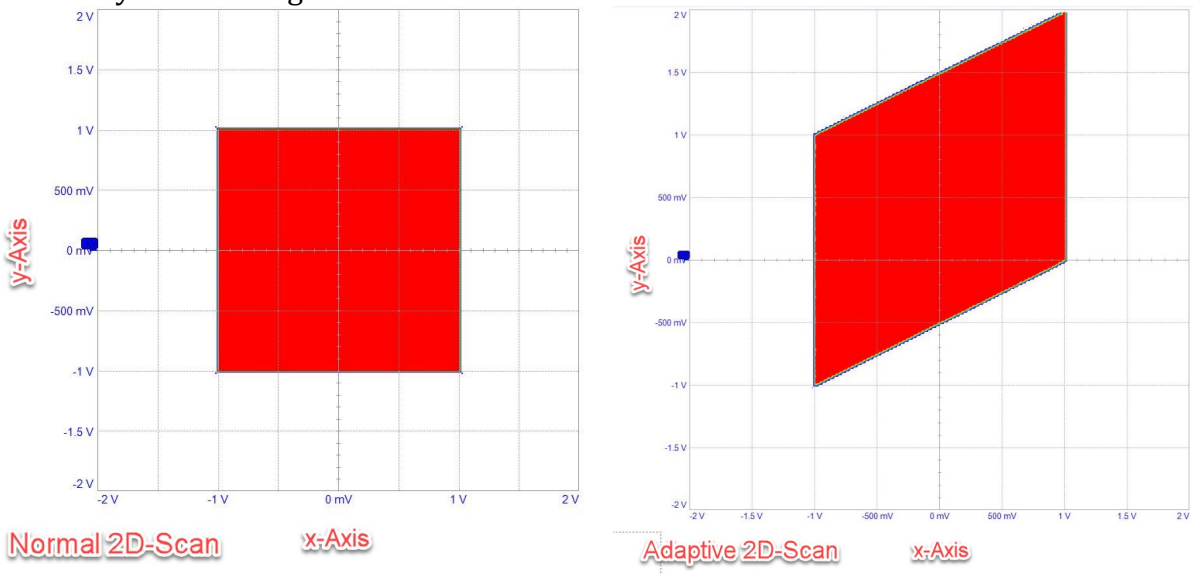
The shiels of the Ethernet cable, the RS-232 cable and the housing of D-Sub the connector for the Digital I/O are directly connected to the housing which is on ground/earth. Also, the reference-ground of the Digital I/O signals are internally connected to the housing (ground/earth). Because the sensitive DAC-Channels are well shielded and isolated from ground/earth, ground loops on these digital signals do not affect the low noise performance of DAC voltages.
For DC bias-voltages or slow ramp-voltages, the low bandwidth (LBW) with a cutoff frequency of 100 Hz offers the advantage of ultra-low noise voltage of only 500 nV_{RMS} in the full ±10 voltage range.

The high bandwidth (HBW) with a cutoff frequency of 100 kHz is intended for high-speed scan voltages or for fast-switching DAC voltages whit a rise/fall-time (10-90%) of only 3.5 µsec, while maintaining a low noise performance of just 4 μV_{RMS}. If required, all the DAC-voltages can be synchronously be updated by an external TTL-signal or by a remote command.

The LNHR DAC II has implemented four independent RAMP/STEP-generators (A, B, C, D) which can be simply programmed by defining the start/stop-voltages and the ramp-time. The shape of the RAMP can be set a "UP-ONLY" (Ramp) or "UP-DOWN" (Triangle).

Further the LNHR DAC II can work as a low noise Arbitrary Waveform Generator (AWG) with 24-bit resolution and an update-rate of up to 100'000 DAC-values per second (update every 10 µsec). Each DAC-Board has two individual AWGs, but both running on the same update rate. The 24 DAC-Channels version has four AWGs (A, B, C, D), each with a maximum memory size of 34'000 AWG points – each AWG point is a 24-bit DAC value. This allows to generate high resolution and low distortion AWG waveforms with frequencies up to maximum 10 kHz (10 AWG points).

By using the STEP-generator in combination with the AWG (programmed with a Ramp-function) two-dimensional scans (2D-Scans) can be generated. Also, adaptive 2D-Scans can be defined where the y-axis gets dependent on the x-axis. Below you can see the xy-plot of two 2D-Scans; both 2D-Scans have a resolution of 1'000 x 1'000 xy-points and a voltage span is ±1 V. The left 2D-Scan is without y-adaption and the right with a y-adaption of 1 mV/x-Step (y-Shift-Voltage); the 1 mV/x-Step multiplied by the 1'000 x-points result in a total y-Shift-Voltage of 1 V:



Note: Avoid overloading the device by sending a large number of remote commands while running 2D-Scans in Auto-Start mode. Otherwise, the 2-Scan can be interrupted.

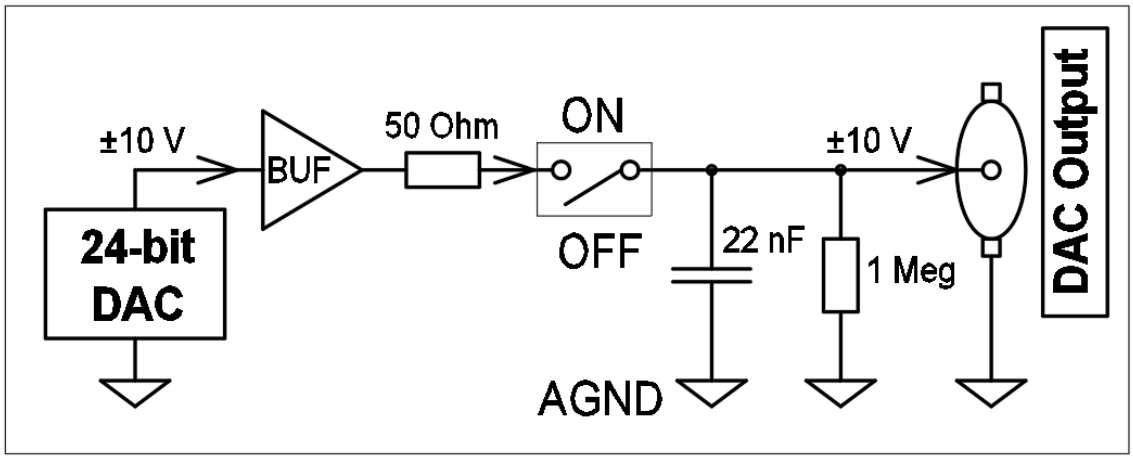
The device can be controlled and programmed by the user-friendly PC-Windows application "LNHR DAC II Commander" which also makes it easy to create such 2D-Scans. Further the device can be controlled remotely by sending/receiving simple ASCII commands via the TCP/IP-network or via the serial port (RS-232). An alpha numeric dot-matrix display (LCD) with 4 x 20 characters in combination with a rotary/push-encoder allows the local control of the device.

7 Output ON/OFF

Each DAC-Channel can be independently switched ON or OFF, after power up all DAC-Channels are in the OFF state. The ON state is indicated on the front-panel by a LED next to the BNC connector; the color of the LED is depending on the selected bandwidth.

In the ON-state the ±10 V DAC output is actively driven via 50 Ohm abled to supply an output current of ±1 mA on all DAC-Channels. On each DAC-Board (Lower and Higher) a single DAC output can be loaded with a maximum output current of ±10 mA. There is no dedicated DAC-Channel, which delivers this higher drive current. But only ONE random DAC channel per DAC-Board can supply up to ±10 mA. Please note that a current of 10 mA already results in a voltage-drop of 500 mV across the 50 Ohm output resistor.

Below the principal diagram of the output stage of a single DAC-Channel in HBW (100 kHz) is given:



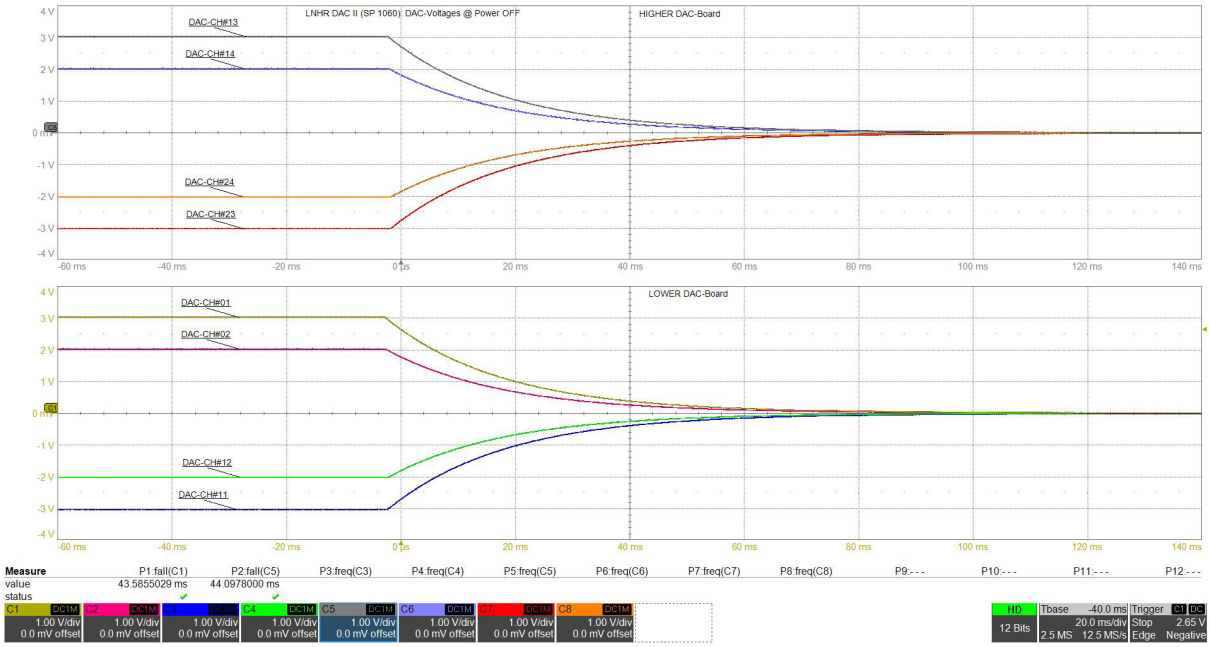
In the OFF state the output gets passively grounded (AGND) by a 1 Mega Ohm resistor in parallel with a 22 nF capacitor. The ON state is indicated on the front-panel by a LED next to the BNC connector; the color of the LED is depending on the selected bandwidth:
Yellow = LBW (100 Hz) / Blue = HBW (100 kHz)

The ON/OFF switch is a high-performance Photo-MOS relay which allows fast and glitch-free switching the DAC output between ON or OFF.

While powering on/off of the device, no spikes are produced on the DAC outputs; this is important since sensitive samples can directly be hooked up to the LNHR DAC II. During the startup phase all the DAC-Channels are in the OFF state by default and the user has to turn them ON by sending the corresponding commands or by using the local LCD and double-click the rotary/push-encoder.

In case of an unintentional power off (blackout), all the DAC voltages are immediately switched to the OFF state and all DAC voltages are passively grounded to reach the save zero voltage after around 100 msec; this is independent of the selected bandwidth. At high-ohmic (>10 Mega Ohm) loads the DAC voltages automatically drop to zero volt with a time-constant of around 22 msec (1 Mega Ohm in parallel with 22 nF); this corresponds to a fall-time (10-90%) of around 48 msec.

The measured decay of eight DAC voltages (four from the Lower and four from the Higher DAC-Board) are shown below when the device gets powered off. The load is 10 Mega Ohm, coming from the oscilloscope (Teledyne/LeCroy, WaveRunner 8108HD) probes:



You can see that the eight DAC voltages decay smoothly (free from any glitches) to zero volts in the event of a blackout of the supply voltage. After about 100 msec the voltages have dropped zero. Therefore, even sensitive samples connected to the LNHR DAC II should not be damaged in the event of a power outage.

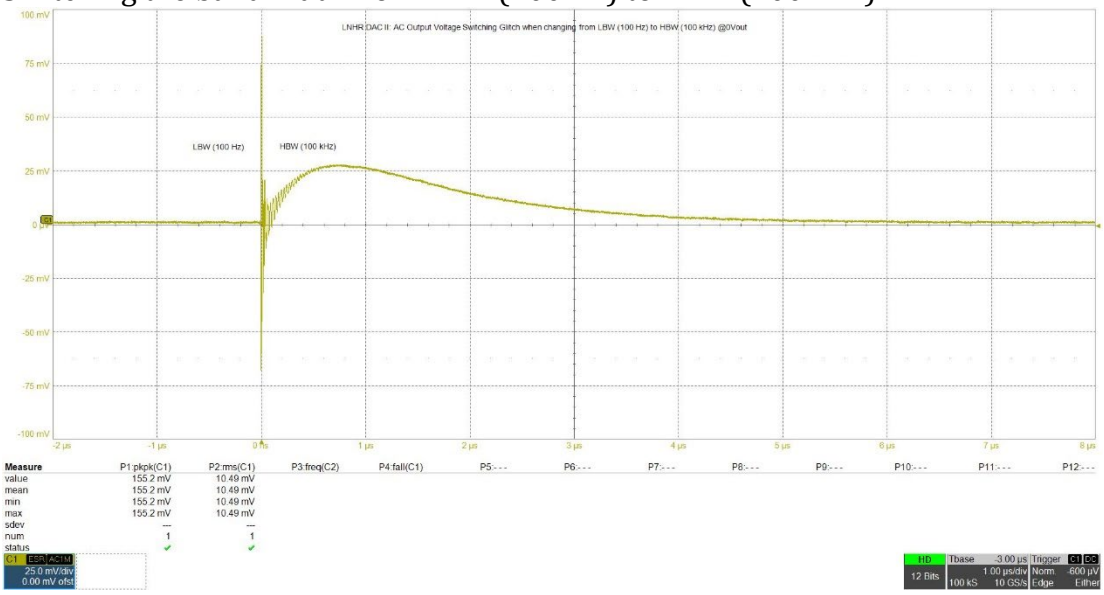
8 Bandwidth LBW (100 Hz) /HBW (100 kHz)

The bandwidth of each DAC output can be individually selected between 100 Hz (LBW) and 100 kHz (HBW). After power-up, all DAC-Channels are in the LWB (100 Hz) mode by default and the user has to select the HBW (100 kHz) by sending the corresponding commands or by using the local LCD and double-click the rotary/push-encoder.

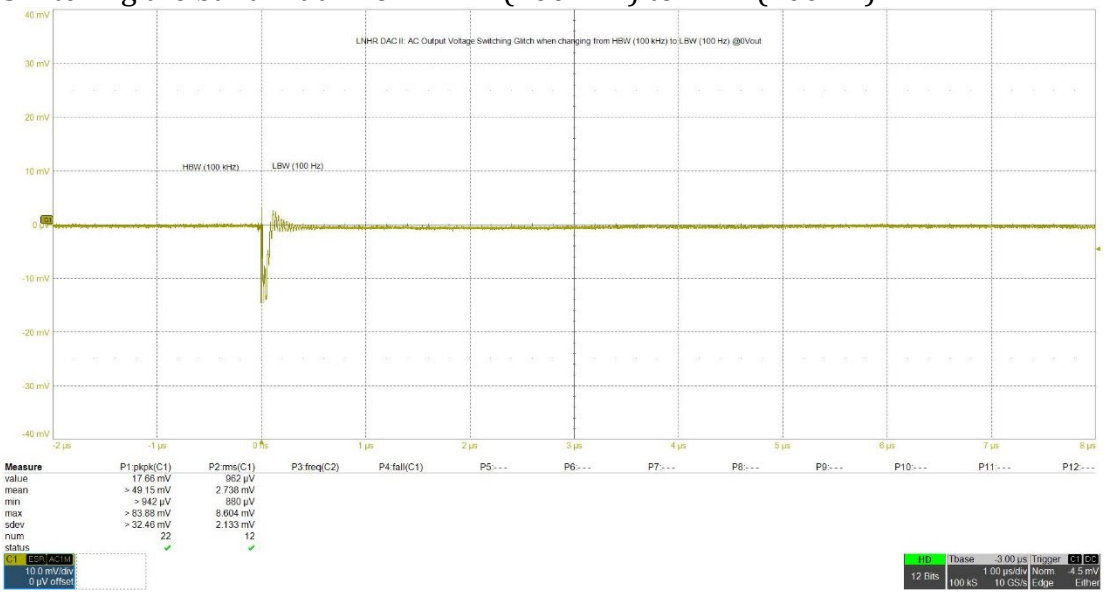
The color of the ON-LED on the front panel is depending on the selected bandwidth:
Yellow = LBW (100 Hz) / Blue = HBW (100 kHz)

CAUTION: When switching the bandwidth, glitch-voltages can occur on the DAC output! Therefore, it is strongly recommended to switch OFF the corresponding DAC-Channel before changing its bandwidth. After switching the bandwidth, wait at least for 0.5 sec before switch ON the DAC-Channel again. When doing so, the bandwidth can be changed safely and glitch-free.

The following typical glitch-voltages can be measured at a turned-on DAC output when switching the bandwidth at 0V output voltage.
Switching the bandwidth from LBW (100 Hz) to HBW (100 kHz):



Switching the bandwidth from HBW (100 kHz) to LBW (100 Hz):



These measurements above show that the glitch-voltages are relatively small and in the higher frequency range (the horizontal scale is 1 µs per division). In many applications such high-frequency glitches are filtered out before it can reach the sample.

However, the following sequence is recommended when the bandwidth needs to be changed while a sensitive sample is connected to the LNHR DAC II:

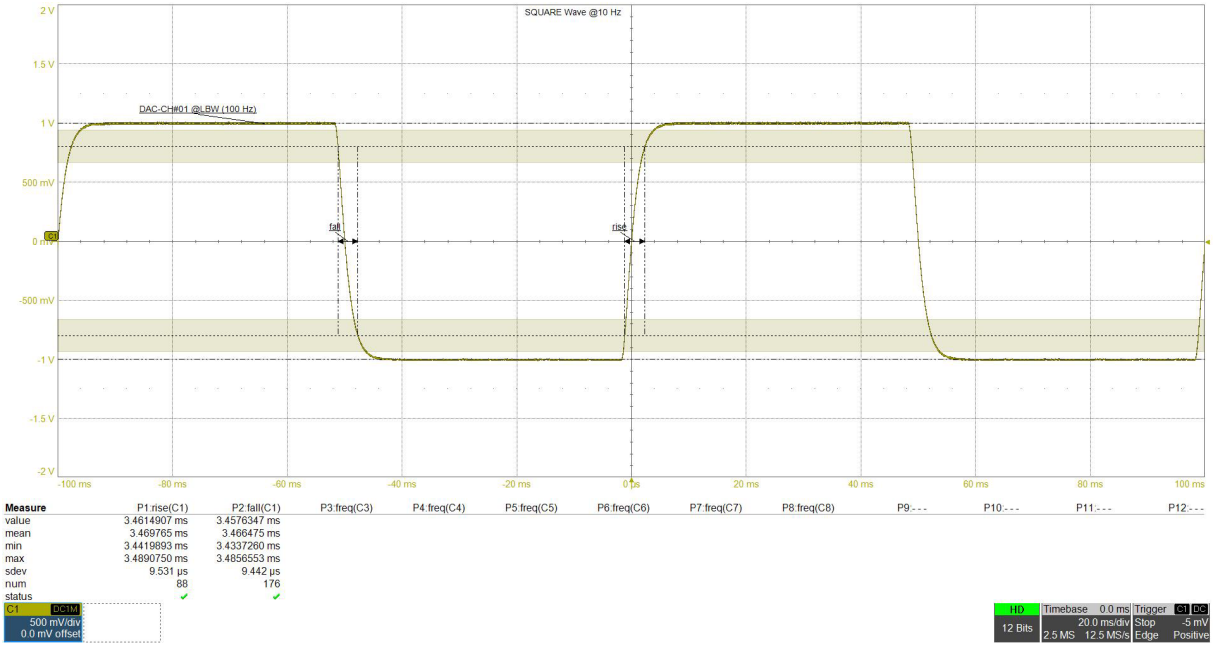
1) Slowly ramp down the DAC voltage to zero (0 V)
2) Switch OFF the DAC-Channel
3) Wait for 100 msec
4) Switch the bandwidth (LBW/HBW)
5) Wait for 500 msec
6) Switch ON the DAC-Channel
7) Slowly ramp up the DAC voltage to its set value

Normally, the bandwidths of all the DAC-Channels are preset by a user's initialization sequence before the DAC-Channels are turned ON and a measurement begins.

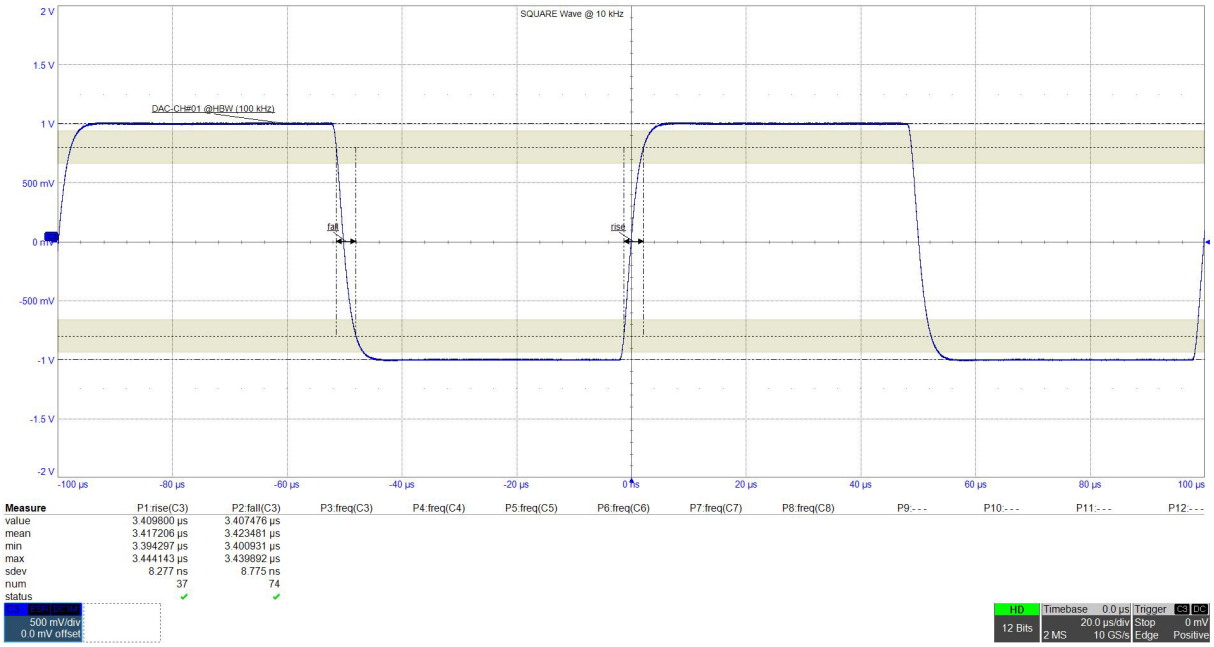
The two different bandwidths are realized by switching the filter-capacitors in the output stage of the DAC. The low-pass (LP) filter is second order filter with critical damping (no overshoot). At the given filter bandwidth, the signal gets reduced by 3 dB; this corresponds to a 70% voltage signal amplitude at a frequency of 100 Hz (LBW) respective at frequency of 100 kHz (HBW). This important to know when signals are generated by using the AWG feature of the LNHR DAC II.

At LBW (100 Hz) the rise/fall-time (10-90%) of the DAC voltage is around 3.5 msec and at HBW (100 kHz) around 3.5 µsec.

An oscilloscope (Teledyne/LeCroy, WaveRunner 8108HD) measurement is shown below, when using **LBW (100 Hz)** while a 10 Hz square wave signal (±1 V) is generated from the internal AWG:



The measurement at LBW (100 Hz) shows no overshoot and a rise/fall-time of around 3.47 msec.
Below, the same measurement is repeated at **HBW (100 kHz)** while a 10 kHz square wave signal (±1 V) is generated from the internal AWG:

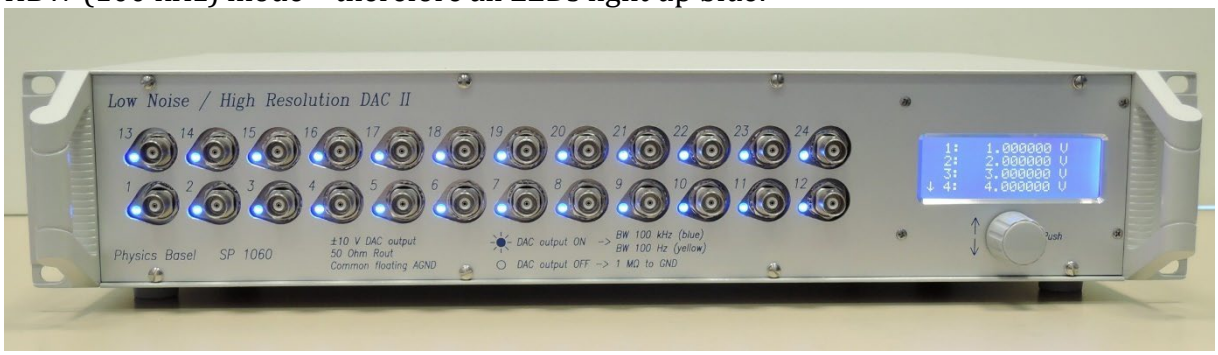


The measurement at HBW (100 kHz) shows no overshoot and a rise/fall-time of around 3.42 µsec.

This LP-filter in the DAC voltage output reduces the broadband noise generated by the DAC. When lowest output noise is demanded, the lower bandwidth (LBW, 100 Hz) must be selected – see chapter “Output Voltage Noise”.

9 Front Panel

The front panel of the LNHR DAC II is shown below with all DAC-Channels switched ON in HBW (100 kHz) mode – therefore all LEDs light up blue:



In the left part, the 24 DAC voltages (±10 V) are routed to the front panel via 24 BNC connectors. The BNC connectors have a horizontal spacing of 25 mm and 21.6 mm in the vertical axis. The outer shields of all the 24 BNC connectors are on the same common floating ground (AGND) which is well isolated from the housing which is on ground/earth. The BNC connectors are mounted on a shielded "Inner Housing" which is galvanically isolated from the housing and the computer interface. The coupling impedance between the AGND and the housing (grounded/earth) is typical >40 Mega Ohm in parallel with a capacitance of around 2.5 nF.

A LED (Yellow/Blue) on the bottom left of the BNC connector indicates the status (ON/OFF) of the associated DAC output:
ON = Actively driven via 50 Ohm: Yellow = LBW (100 Hz) / Blue = HBW (100 kHz)
OFF = Passively grounded via 1 Mega Ohm in parallel with 22 nF

The large front panel recesses for the 24 BNC connectors make sure that the outer shields don't make an electrical contact to the housing which is on ground/earth. Make sure that the outer shells of the attached BNC cables don't touch the front panel and that no conductive parts are trapped between the front panel and the inner-housing. This would destroy the galvanic isolation and thus lead to ground-loop problems.

All the ±10 V DAC voltages can source up to ±1 mA output current; this corresponds to a load resistance of 10 kOhm when using the full voltage range of ±10 V. On each DAC-Board (Lower = CH1…12 and Higher = CH13…24) a single random DAC output can be loaded with a maximum output current of ±10 mA (corresponding to a 1 kOhm load resistance).

The common floating ground of all the DAC voltages (outer shield of the BNCs) can be shifted up to ±20 V with respect to the housing/earth, by applying an external bias voltage. This bias voltage has to be connected to the BNC connector on the back panel (see chapter "Back Panel").

The LC-Display and the rotary/push knob (encoder) are located on the right side of the front panel. These components allow local control of the LNHR DAC II; only basic manipulations and settings can be done locally. Fully access is given by the remote control via ASCII commands or by using the Windows application "LNHR DAC II Commander". For further information see the "LNHR DAC II Programmer's Manual" and the "LNHR DAC II Commander Description".

9.1 Local Control

By using LC-Display and the rotary/push knob (encoder) basic settings and readouts can be performed locally.

9.1.1 Startup Displays

After the power switch is turned ON (on back panel) the device starts up and the following message is displayed on the LCD:

```
    W E L C O M E
  Now starting the
LNHR DAC II software
(takes about 45 sec)
```

After around 45 seconds the boot process has finished and this message appears on the LCD:

```
Software started!

Now, initializing
the Hardware...
```

Shortly later, the number of detected DAC-Channels (12 or 24) and the device type are displayed:

```
 24 DAC-CHs detected
 LNHR DAC II RMP/AWG
    Physics Basel
       SP 1060
```

9.1.2 Main Menu

After 10 seconds or when pressing the push button, the Main Menu gets displayed on the LCD. With the rotary knob the Main Menu can be scrolled up and down. One of the 16 Menu Items can be selected by short pressing the push-button. Leaving a sub-menu is done by long (> 1 sec) pressing the push-button:

```
Show/Edit: Voltage
Show/Edit: DEC-VALs
Show/Edit: HEX-VALs
Show/Edit: BWs
Edit: ALL DAC-CHs
Show: DAC-MODEs
Show: Temperatures
Show: CPU-Load
Show: Power-Status
RS-232 Settings
TCP/IP Settings
Software Release
Hardware Version
Restart the device
Contact Information
HELP
```

9.1.3 Show/Edit: Voltage

Under this Menu Item the DAC-Voltages can be displayed and modified. After power up all DAC-Channels are switched OFF and therefore the display is <OFF>. By selecting a DAC-Channel (scrolling up/down) followed by a double-click, the corresponding DAC-Channel is switched ON and its actual voltage is displayed. A double-click on an active (ON) DAC-Channel switches it OFF again.
The DAC voltage can be set by selecting a digit and then pressing the push button; then the voltage at the selected digit can be increase/decrease by using the rotary knob:

```
  1:   -0.000000 V
  2:   <OFF>
  3:    3.333333 V
v 4: -10.000000 V
```

The displayed voltages are not measured; they are calculated from the set DAC values. Since the absolute DAC output voltage has a typical accuracy of ±200 µV, the shown voltages may be slightly different to the real DAC output voltages.

Due to the intrinsic DAC resolution of 1.192093 µV the last digit (µV) may skip some values due to rounding to the nearest possible output voltage.

9.1.4 Show/Edit: DEC-VALs

The decimal DAC-Values can be displayed and modified in a range from 0 (-10.000000 V) to 16'777'215 (+10.000000 V). The editing of a DAC-Value follows the same rules as described above under "Show/Edit: Voltage".
The resolution of the last digit corresponds to a voltage step of 1.192093 µV:

```
  1:    8388607
  2:   <OFF>
  3:   11184810
v 4:          0
```

For converting a decimal DAC-Value to a DAC-Voltage, see the chapter "Converting DAC-Voltage to DAC-Value".

9.1.5 Show/Edit: HEX-VALs

The hexadecimal DAC-Values can be displayed and modified in a range from 0x000000 (-10.000000 V) to 0xFFFFFF (+10.000000 V). The editing of a DAC-Value follows the same rules as described above under "Show/Edit: Voltage".
The resolution of the last digit corresponds to a voltage step of 1.192093 µV:

```
  1:   0x7FFFFF
  2:   <OFF>
  3:   0xAAAAAA
v 4:   0x000000
```

For converting a hexadecimal DAC-Value to a DAC-Voltage, see the chapter "Converting DAC-Voltage to DAC-Value".

9.1.6 Show/Edit: BWs

Under this Menu Item the Bandwidth of the DAC-Channels can be displayed and modified. For each DAC-Channel the Bandwidth can be individually switched between LBW (100

Hz) and HBW (100 kHz). The Bandwidth of a selected DAC-Channel can be toggled between LBW (100 Hz) and HBW (100 kHz) by a double-click.
CAUTION: To prevent from glitch-voltages, first switch OFF the corresponding DAC-Channel before switching the Bandwidth!

```
  1:  LBW (100 Hz)
  2:  HBW (100 kHz)
  3:  LBW (100 Hz)
v 4:  HBW (100 kHz)
```

The color of the ON-LED on the front panel is depending on the selected Bandwidth:
Yellow = LBW (100 Hz) / Blue = HBW (100 kHz)

9.1.7 Edit: ALL DAC-CHs

All DAC-Channels can be simultaneously set to a DAC-Voltage, alter its Bandwidth between LBW and HBW and switch them ON or OFF.
All DAC-Voltages are modified by selecting the line "Vout". The editing of a DAC-Value follows the same rules as described above under "Show/Edit: Voltage".
To modify all Bandwidths, navigate to the line "<LBW> / <HBW>" and set the cursor to the demanded Bandwidth and then make a double-click.
CAUTION: To prevent from glitch-voltages, first switch OFF ALL the DAC-Channels before switching ALL the Bandwidths!
For switching all DAC-Channels ON or OFF, navigate to the line "<OFF> / <ON>" and set the cursor to the demanded output-state and then make a double-click.

```
Set ALL DAC-CHs:
  Vout: -10.000000 V
 <LBW> / <HBW>
 <OFF> / <ON>
```

9.1.8 Show: DAC-MODEs

The DAC-MODEs can be display under this Menu Item. The following different DAC-Modes can be displayed:
"DAC (normal)", "<SYNC>", "<RMP-STP>", "<AWG>", "<ERR>", "<--->" (not available)

```
  1:  DAC (normal)
  2:  DAC (normal)
  3:  <RMP-STP>
v 4:  <AWG>
```

9.1.9 Show: Temperatures

The Temperatures of the two DAC-Boards (Lower/Higher DAC-Board), of the Microcontroller-Board and of the CPU/FPGA can be readout under this Menu Item:

```
Hi DAC-Board: 39.2°C
Lo DAC-Board: 38.0°C
µC-Board    : 43.6°C
CPU/FPGA    : 49.2°C
```

Note: A running AWG and the "AWG Only" mode disables the Temperature measurement on the corresponding DAC-Board; then the temperature is displayed with "NaN°C".

The Temperatures of the two DAC-Boards and the Microcontroller-Board must be below 70°C; the Temperature of the CPU/FPGA must be below 90°C.

9.1.10 Show: CPU-Load

The actual CPU-Load and its Status can be displayed under this Menu Item. The typical CPU-Load is between 40% and 75%. Up to a CPU-Load of 75% the Status is "Normal"; between 75% and 85% it is "High", between 85% and 95% it is "Very High". For a CPU-Load >95% the system gets overloaded the Status is "Extremely High!" and the following warning is shown: "Warning: OVERLOADED! Reduce RMP/STP-CHs".

```
CPU-Load: 41%
Status  : Normal
```

9.1.11 Show: Power-Status

The Status of the three supply voltages is indicated here – all must be OK:

```
+24 Vc Supply: OK
+15 Va Supply: OK
-15 Va Supply: OK
```

If one of the supply voltages falls below its threshold, all DAC-Channels are switched OFF immediately and they drop to zero volt with a time-constant of around 22 msec. See chapter "Output ON/OFF".

9.1.12 RS-232 Settings

The Baud rate of the serial connection can be set in this Menu Item. Baud rates from to 300 up to 115'200 (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bit/sec) can be selected by turning the rotary knob. At delivery a Baud rate of 9'600 is programmed.
The data length of 8 bit, the number of stop-bits (1 stop) and the parity (none) are fixed and cannot be changed:

```
Baud rate: 9600
 (300-115200 bits/s)
Fix: 8 data, 1 stop
no parity, XON/XOFF
```

When the Baud rate has been changed by the user and the button is pressed, the device asks what to do. With the rotary knob one can chose between two options: "Escape to MAIN MENU" makes no changes and the old Baud rate remains valid. When choosing "Use/Save Baud Rate!" the new Baud rate gets activated and it is saved permanently:

```
WHAT TO DO NOW?
 Escape to MAIN MENU
 Use/Save Baud Rate!
```

9.1.13 TCP/IP Settings

Under this Menu Item the IP-Address and the Subnet-Mask of the device can be programmed. At delivery the private IP-Address 192.168.000.005 with a subnet-mask of 255.255.255.000 is programmed. Setting a different IP-address or a subnet-mask can be done in the same way as editing a DAC-Value:

```
IP-Address:
     192.168.000.005
Subnet-Mask:
     255.255.255.000
```

After setting new IP-values and long pressing the push button the device asks what to do. With the rotary knob one can select between two options: "Escape to MAIN MENU" makes no changes and the old IP-Address and Subnet-Mask remains valid. When selecting "Save IP & Restart!" the modified values are saved permanently and the device is restarted (takes about 45 seconds). Thereafter the new IP-Settings are active:

```
WHAT TO DO NOW?
 Escape to MAIN MENU
 Save IP & Restart!
```

When selecting the menu item "Save IP & Restart!" the following display appears:

```
Writing TCP/IP-ADR
and Subnet-Mask...

         Please wait!
```

After a while the device gets restarted automatically and shows the following message:

```
Restarting now...


         Please wait!
```

Note: During the restart of the device, all DAC channels are switched OFF and they are reset to an output voltage of zero (0 V).

9.1.14 Software Release

This Menu Item allows to readout the Software Release installed on the LNHR DAC II. By scrolling down further information can be displayed:

```
SOFTWARE RELEASE:
Revision 3.4.9q
(c) Physics, StM
University Basel
May 2022.
Code generated by
Using LabVIEW 2018
with FPGA and RT
software modules.
```

9.1.15 Hardware Version

Hardware Version and some other information can be recalled by this Menu Item – use the rotary knob to scroll through this information:

```
LNHR DAC II SP 1060
HARDWARE VERSION:
SN 10600000001
24 DAC-Channels
DAC-Board:  Rev 2.0
REF-Board:  Rev 1.3
ADA-Board:  Rev 1.0
PWR-Supply: Rev 1.0
µC/FPGA: sbRIO-9607
NI, 2xARM A9@667MHz
HDB-CAL: 14.12.2021
LDB-CAL: 13.12.2021
```

At the very end you can find date of the last calibration of the two DAC-Boards (HDB: Higher DAC-Board with CH 13…CH 24 / LDB: Lower DAC-Board with CH 1…CH 12). The format of the date is DD.MM.YYYY.

9.1.16 Restart the device

Here you can restart the device without using the power ON/OFF switch on the back panel. In addition, the TCP/IP-Telnet connection can be restarted. An open Telnet connection is forced to closed; this can be useful if the host computer has crashed.
Under this menu item you can choose between “Escape to MAIN MENU”, “Restart device now!” and “Restart Telnet now!”:

```
WHAT TO DO NOW?
 Escape to MAIN MENU
 Restart device now!
 Restart Telnet now!
```

If “Escape to MAIN MENU” is selected, nothing will be restarted and the software returns to the main menu.

If “Restart device now!” is selected, the following message will pop up and after a while (several seconds) the reboot process will be started:

```
Restarting now...


         Please wait!
```

Note: During the restart of the device, all DAC channels are switched OFF and they are reset to an output voltage of zero (0 V).

If “Restart Telnet now!” is chosen, an open TCP/IP-Telnet connection is closed immediately and the software returns to the main menu; the process is very fast and no further information is displayed.

Note: The status of the device is not affected by closing the Telnet connection and all the DAC output voltages are unaffected.

If a TCP/IP-Telnet connection isn't properly closed by the host computer due to a crash or by an interrupted Ethernet connection, the Telnet connection on the LNHR DAC II may still be open. Since only one Telnet connection can be open on the device, the previous one must be closed first, otherwise no new Telnet communication can be established. In this case, the user must manually close the TCP/IP-Telnet connection via this "Restart Telnet now!" menu item.

9.1.17 Contact Information

The contact details can be called up via this Menu Item – in case of problem you can contact the manufacturer:

```
CONTACT INFORMATION:
University Basel
Dep. Of Physics
Michael Steinacher
Lab. 2.17
Klingelbergstr. 82
CH-4056 Basel
Switzerland
```

9.1.18 HELP

Some helpful and compressed information can be found in this Menu Item:

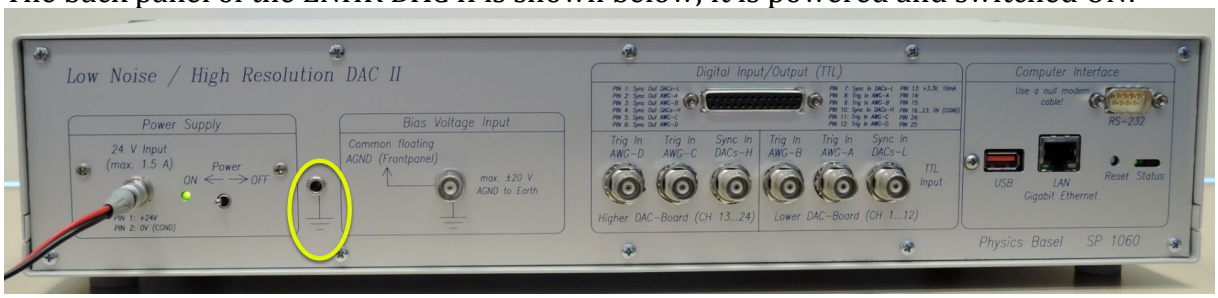
```
HELP: 3.4.9
This 12/24-CH DAC
Can be controlled
by four different
sources:

1) Locally by using
the LCD, the rotary
knob and its push
button:            v
```

Use the rotary knob to scroll through the complete help text.

10 Back Panel

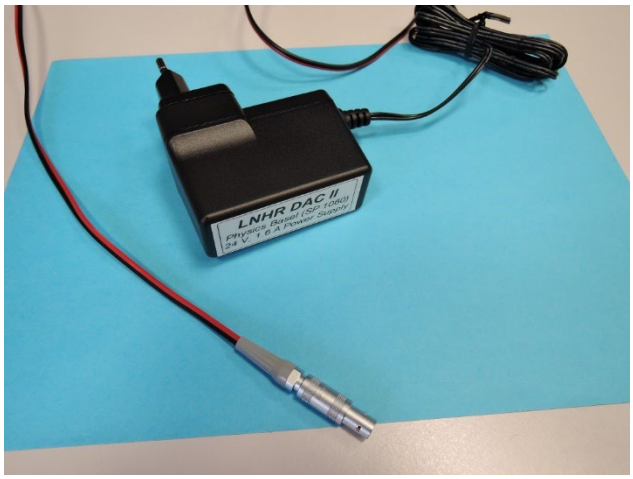
The back panel of the LNHR DAC II is shown below; it is powered and switched ON:



Warning: For safety reasons, make sure that the housing of the device is always connected to ground/earth. When not mounted in a grounded 19" rack, use the 4 mm banana ground jack on the back panel to connect the housing to a proper ground/earth.

10.1 Power Supply

To minimize the electromagnetic interference from the power supply to the sensitive DAC outputs, the LNHR DAC II is supplied by an external 24 V_{DC} power-supply. A suitable wall-plug power adapter is included in the delivery. It is a 40 W / 24 V medical switching power-supply with a rated current of maximum 1.66 A; the type is GEM40I24 from the company MeanWell. With its output cable length of 3 meters the power-supply can be in well distance from the sensitive device:



The LNHR DAC II can also be supplied from other clean 24 V_{DC} sources, including batteries. The nominal 24 V_{DC} voltage must be within a tolerance of ±10 % and the device draws at maximum a current of 1.5 A_{DC}. The needed power-plug is a 2-pin LEMO (type FFA.0S.302.CLAL44Z) with pin 1 connected to +24 V and pin 2 connected to 0 V.

The Power ON/OFF switch near the power jack allows to switch the device ON or OFF; if switched OFF no supply-current is flowing. The green LED between the switch and the power jack indicates when the device is powered ON with a valid supply voltage.

10.2 Bias Voltage Input

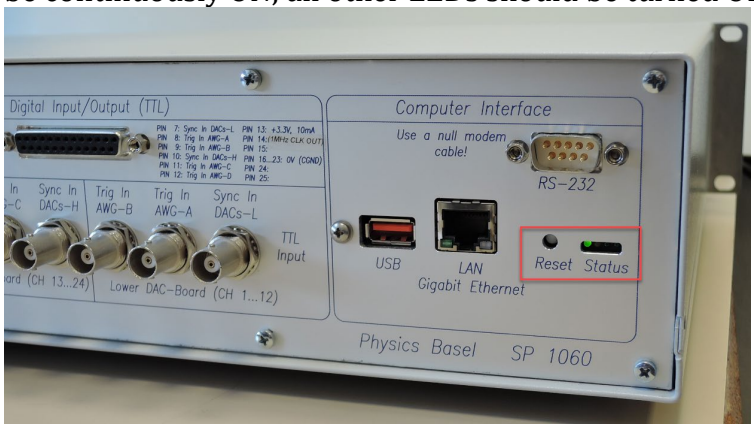
Via the external Bias Voltage Input (BNC connector) the common floating ground (AGND) of all the DAC voltages can be shifted up to ±20 V with respect to the housing/earth; it is internally restricted to ±25 V by Zener-Diodes.

Note: When applying a Bias Voltage, the common analog ground (AGND) of all the DAC outputs is no longer floating and ground-loops may significantly degrade the noise-performance of the device. Under normal operation leave this Bias Voltage Input unconnected (open).

10.3 Reset & Status LEDs

The device can be reset by shortly press the "Reset" push button with a small screwdriver through the back panel. Doing so the LNHR DAC II will be restarted immediately.
Note: During the restart of the device, all DAC channels are switched OFF and they are reset to an output voltage of zero (0 V).

After the device has successfully booted the most left green LED in the Status display must be continuously ON; all other LEDs should be turned OFF:



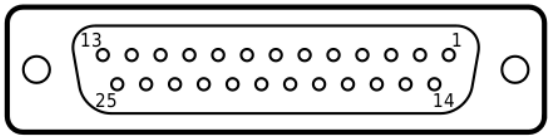
10.4 Remote Control Connectors

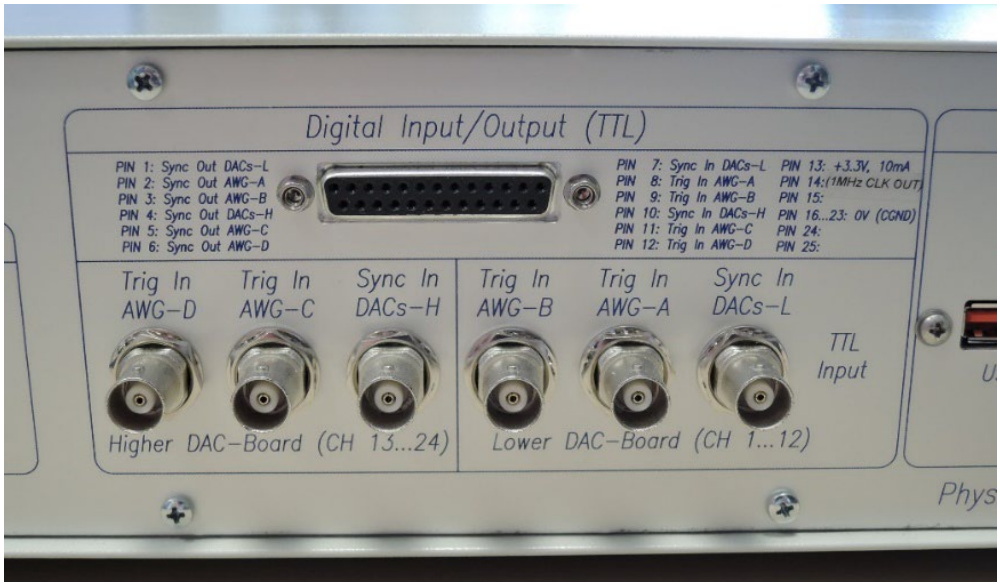
The connectors for the remote control (RS-232 or Ethernet) are located on the right. The Ethernet port of the LNHR DAC II can be directly connected to a computer, a crossover cable isn't needed. For the serial interface (RS-232) a null modem cable (female-female) has to be used; such a RS-232 cable with a length of 3 meters is delivered with the device. For further information see the "LNHR DAC II Programmer's Manual".
Note: The USB connection cannot be used for remote control. The shiels of the Ethernet cable and the RS-232 cable are connected to the housing which is on ground/earth.

10.5 Digital Input/Output (TTL)

By using the Digital Input/Output the LNHR DAC II can be easily connected to other devices in a complex and synchronized measurement setup. This allows fast and precise synchronization and triggering. For example, all DAC-Channels can be updated simultaneously on the rising-edge of an external TTL signal. The four AWGs can

individually be started (and stopped) or clocked (Single-Step) by and external TTL trigger signal. The AGWs generate four synchronization output signals for triggering other devices.
The Digital Input/Output are referenced to the computer-ground (CGND) which is internally connected to the grounded housing. If a ground-decoupling is needed, the +3.3 V supply voltage output allows simple isolation via opto-couplers. The +3.3 V output voltage can drive continuously 10 mA and 50 mA peak current.
The Digital Input/Output-levels are TTL compatible and the Digital Inputs are +5 V tolerant:





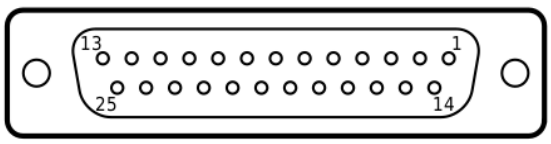
Warning: Do not apply input voltages outside the maximum range of 0 V to +5 V. Otherwise, the device can be damaged!

All Digital Inputs are pulled-down by a 10 kOhm resistor; therefore, all open inputs are on a low-level. The Digital Outputs deliver a typical high-level of +3.3 V and a typical low-level of +0.1 V; these levels are reached when no output current is flowing. The output resistance is 100 Ohm and a maximum output current of ±5 mA can be source/sink from each of the Digital Outputs.
All Digital Input/Output are accessible via the D-Sub 25-pin female connector. The six Digital Inputs for Triggering and Synchronization are also wired in parallel to six BNC connectors; this allows the user to easily plug in their Synchronization- and Trigger-signals. In the left part the input signals for the "Higher DAC-Board (CH 13...24)" are located and in the right part the signals for the "Lower DAC-Board (CH 1...12)".

Warning: Do not drive the Digital Inputs on the D-Sub connector while the BNC-Inputs are connected to another signal source, since the two different inputs are internally interconnected!

Below the pinout of the D-SUB 25-pin connector is given; the six Digital Inputs printed in bold are wired in parallel to the six BNC connectors:

Pinout of D-SUB 25-pin: Digital Input/Output (TTL)			
PIN	Input/Output	Signal Name	Description
1	Output	Sync Out DACs-L	Rising-edge indicates that the DACs on Lower DAC-Board are updated (in "Instantly Mode" always High)
2	Output	Sync Out AWG-A	Sync-signal from AWG A on Lower DAC-Board (High for the first 50% of AWG A-Memory Size)
3	Output	Sync Out AWG-B	Sync-signal from AWG B on Lower DAC-Board (High for the first 50% of AWG B-Memory Size)
4	Output	Sync Out DACs-H	Rising-edge indicates that the DACs on Higher DAC-Board are updated (in "Instantly Mode" always High)
5	Output	Sync Out AWG-C	Sync-signal from AWG C on Higher DAC-Board (High for the first 50% of AWG C-Memory Size)
6	Output	Sync Out AWG-D	Sync-signal from AWG D on Higher DAC-Board (High for the first 50% of AWG D-Memory Size)
7	**Input**	**Sync In DACs-L**	**Synchronized update of all the DACs on Lower DAC-Board (on rising-edge, only in "External SYNC Mode")**
8	**Input**	**Trig In AWG-A**	**External control of the AWG-A on Lower DAC-Board: Start/Single-Step (rising-edge), [Stop (falling-edge)]**
9	**Input**	**Trig In AWG-B**	**External control of the AWG-B on Lower DAC-Board: Start/Single-Step (rising-edge), [Stop (falling-edge)]**
10	**Input**	**Sync In DACs-H**	**Synchronized update of all the DACs on Higher DAC-Board (on rising-edge, only in "External SYNC Mode")**
11	**Input**	**Trig In AWG-C**	**External control of the AWG-C on Higher DAC-Board: Start/Single-Step (rising-edge), [Stop (falling-edge)]**
12	**Input**	**Trig In AWG-D**	**External control of the AWG-D on Higher DAC-Board: Start/Single-Step (rising-edge), [Stop (falling-edge)]**
13	Power Output	+3.3V, 10mA	+3.3V Supply voltage output, 10 mA (for Opto-Couplers)
14	(Output)	(1MHz CLKout)	1 MHz Reference Clock Output with 50% duty-cycle (for synchronization with other devices) - must be activated!
15	GND (Output)	0V (SPARE_2_OUT)	CGND (SPARE_2_OUT, not used)
16	GND	0V	CGND
17	GND	0V	CGND
18	GND	0V	CGND
19	GND	0V	CGND
20	GND	0V	CGND
21	GND	0V	CGND
22	GND	0V	CGND
23	GND	0V	CGND
24	GND (Input)	0V (SPARE_1_IN)	CGND (SPARE_1_IN, not used)
25	GND (Input)	0V (SPARE_2_IN)	CGND (SPARE_2_IN, not used)

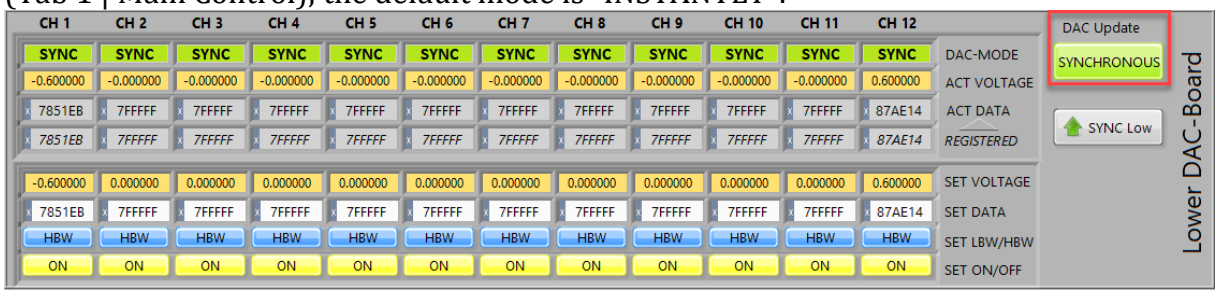


This pinout is also indicated on the back panel on both sides of the D-SUB connector. The ground-reference of these digital signals is the computer-ground (CGND) which is internally connected to the grounded housing.

10.5.1 External DAC Synchronization

All DAC-Channels of one DAC-Board can be updated synchronously by an external TTL signal, applied to the "Sync In DACs-L" input (for the Lower DAC-Board with CH 1..12) or the "Sync In DACs-H" input (for the Higher DAC-Board with CH 13...24). If all 24 DAC-Channels on both DAC-Boards should be updated synchronously, connect the same TTL signal to both of the synchronization inputs. The synchronous update is performed on the rising edge of the external TTL signal.

For a synchronous DAC update the DAC-Board must by in "SYNCHRONOUS" mode which can be set via a remote command or by using the "LNHR DAC II Commander" application (Tab 1 | Main Control); the default mode is "INSTANTLY":

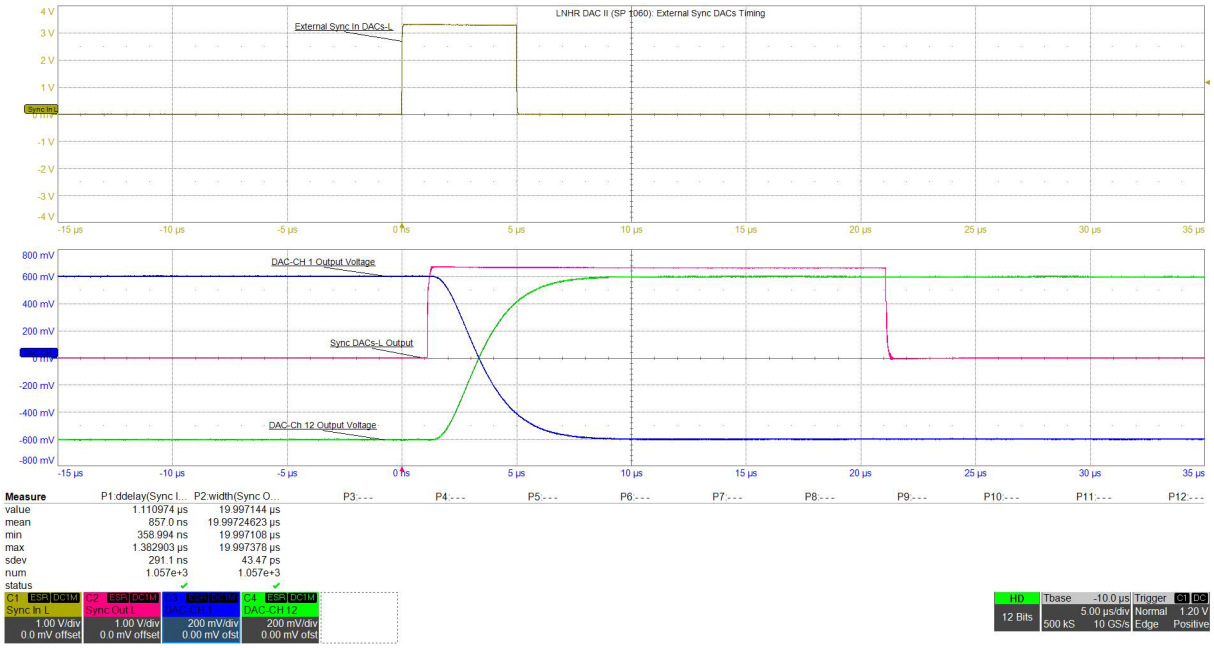


Each DAC-Board can be individually set to "SYNCHRONOUS" or "INSTANTLY" mode and therefore two separate digital synchronization-inputs (BNC connectors) exist on the back panel.

If the DAC-Board is in the "INSTANTLY" mode, the "REGISTERED DATA" is immediately transferred to the "ACTUAL DATA" which instantly updates the DAC output voltage.
In the "INSTANTLY" mode, the "Sync In DACs" input is ignored and the "Sync Out DACs" output is always high.

In the "SYNCHRONOUS" mode the "REGISTERED DATA" is transferred to the "ACTUAL DATA" on SYNC-event only. Such SYNC-event has the following three sources: A rising-edge on the external "Sync In DACs" input TTL signal; an ASCI synchronization command received from the remote control (via Ethernet or RS-232); a presses "SYNC" button in the "LNHR DAC II Commander" application.
In the "SYNCHRONOUS" mode, the "Sync In DACs" input is active and the "Sync Out DACs" output is low until a SYNC-event is detected; then a pulse with a fixed length of 20 µsec is released on the "Sync Out DACs" output.

Below the timing with an external synchronization signal on "Sync In DACs-L" (top grid, yellow) on the Lower DAC-Board is shown. On the bottom grid the "Sync Out DACs-L" output signal (red) and the two DAC output voltages (blue and green) are measured. The output voltage of the DAC-Channel 1 changes from +600 mV to -600 mV and the DAC-Channel 12 from -600 mV to +600 mV. Both channels are set to HBW (100 kHz) and it takes around 10 µsec until the new DAC voltages are settled. The update of the DAC outputs is on the rising-edge of the external "Sync In DACs" TTL input signal:



The minimum pulse-width of the “Sync In DACs” TTL input signal is 2 µsec and the maximum repetition frequency is 40 kHz (every 25 µsec).

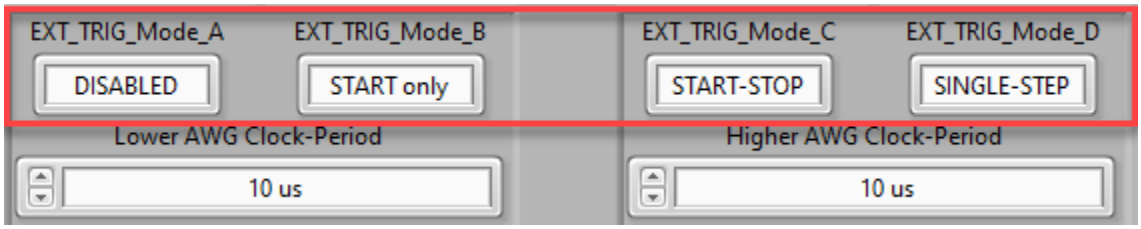
The time delay from the rising-edge of the external “Sync In DACs” input to the rising-edge of the “Sync Out DACs” output signal (which updates the DAC outputs) is typical 0.9 µsec. The actual time-delay varies between 0.4 µsec and 1.4 µsec; this corresponds to a time-jitter of 1 µsec.

The “Sync Out DACs” output signal has a fixed pulse-width of 20 µsec and it is also generated when a synchronization command is received from the remote control or the user presses the “SYNC” button in the “LNHR DAC II Commander” application.

10.5.2 External AWG Trigger

The four AWGs (A, B, C, D) can be triggered (started/stopped/stepped) by an external TTL signal applied to the “Trig In AWG-A, B, C, D” input. If multiple AWGs are to be controlled synchronously, connect the same TTL signal to the appropriate "Trig In AWG" inputs.

The behavior of the external AWG Trigger input signals can be programmed by a remote command or by using the “LNHR DAC II Commander” application (Tab 3 | AWG Control); the default mode is “DISABLED”:

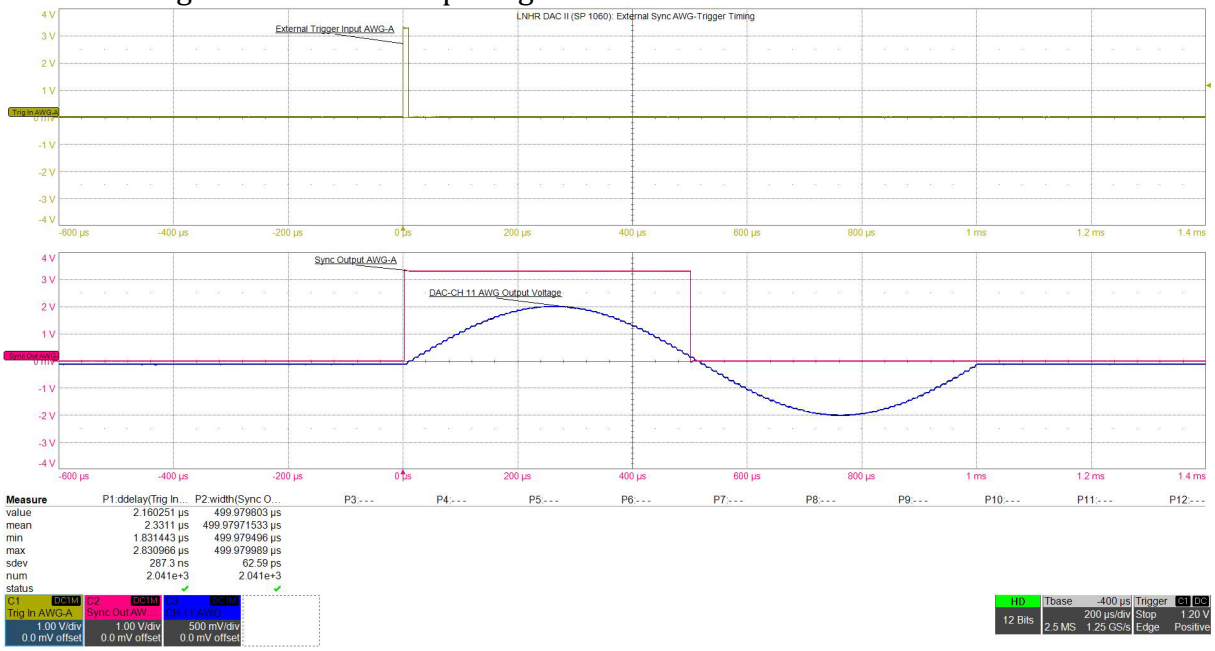


Each of the four AWGs (A, B, C, D) has its own programmable mode-register and there are four digital trigger-inputs (BNC connectors) on the back panel.

In the “DISABLED” mode, the external AWG Trigger input signal is ignored.
In the “START only” mode, the AWG is started on the rising-edge of the AWG Trigger input.

In the “START-STOP” mode, the AWG is started on the rising-edge and stopped on the falling-edge of the external AWG Trigger input signal; the AWG runs during the external AWG Trigger input is high.
In the “SINGLE-STEP” mode, the AWG gets clocked on the rising edge of the external input; the frequency is from DC up to 100 kHz and the minimum pulse-width is 2 µsec. This mode allows stepping through the AWG values synchronized with an external trigger signal.

Below the timing in the “START only” mode with an external 10 µsec triggering signal on “Trig In AWG-A” (top grid, yellow) is shown. The AWG-A is predefined on DAC-CH 11 with a single-cycle 1 kHz sinusoidal signal consisting of 100 points. On the bottom grid the “Sync Out AWG-A” output signal (red) and the AWG output voltage (blue) on DAC-CH 11 set to HBW (100 kHz) is measured. The start of the AWG-A is on the rising-edge of the external “Trig In AWG-A” TTL input signal:

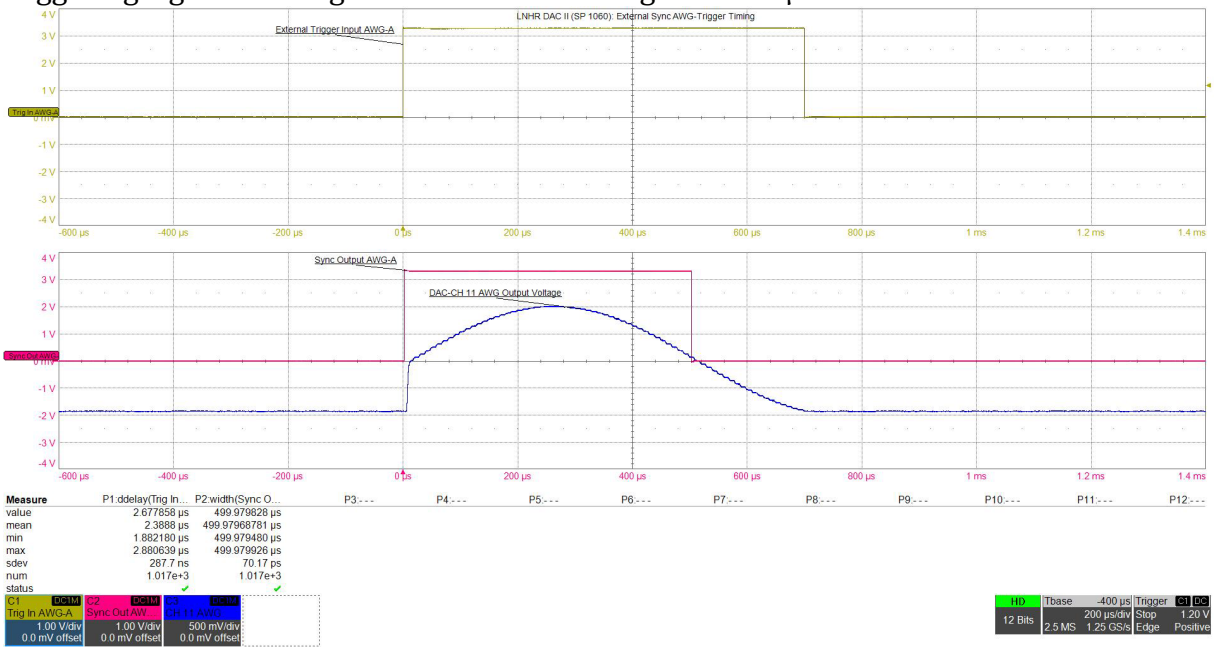


The minimum pulse-width of the “Trig In AWG” TTL input signal is 2 µsec and the maximum repetition frequency is 40 kHz (every 25 µsec).

The time delay from the rising-edge of the external “Trig In AWG” input to the rising-edge of the “Sync Out AWG” output signal (which indicates the start of the AWG) is typical 2.3 µsec. The actual time-delay varies between 1.8 µsec and 2.8 µsec; this corresponds to a time-jitter of 1 µsec. From the rising-edge of “Sync Out AWG” output signal until the first AWG point arrives on the DAC output takes again around 4 µsec. Therefore, the total time delay from the rising-edge of the external “Trig In AWG” to the first AWG point converted to a DAC voltage is around 6.3 µsec.

The “Sync Out AWG-A” output signal is high for the first half of the AGW-points (50% duty-cycle); therefore, in our example it has a pulse-width of 500 µsec. The “Sync Out AWG” output signals are also generated when an AWG start command is received from the remote control or the user presses the “Start AWG” button in the “LNHR DAC II Commander” application. As soon as the AWG is stopped, the corresponding “Sync Out AWG” output signal is set low.

For the same AWG-signal the timing in the “START-STOP” mode with an external triggering signal on “Trig In AWG-A” with a length of 700 µsec is shown below:

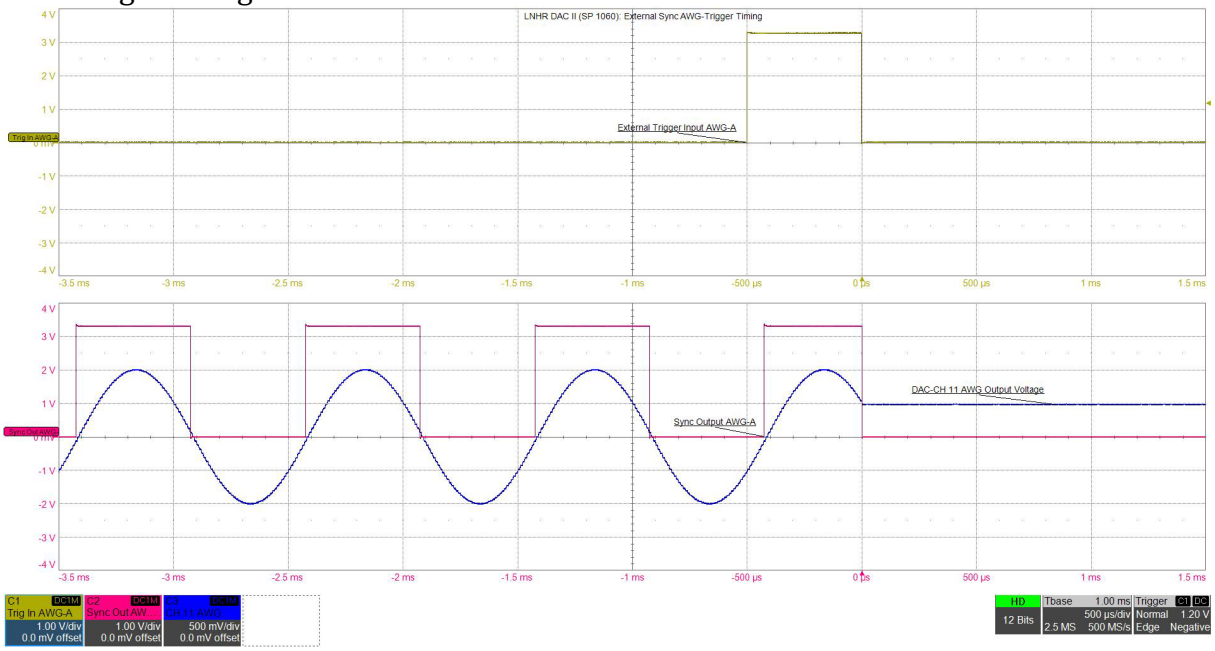


The rising-edge starts the AWG while the falling-edge stops the AWG after 700 µsec. Since this is longer than the first half of the AGW-points the “Sync Out AWG-A” output signal has sill a pulse-width of 500 µsec.

With the same setup, the result with an external triggering signal on “Trig In AWG-A” with a length of only 400 µsec is shown below:

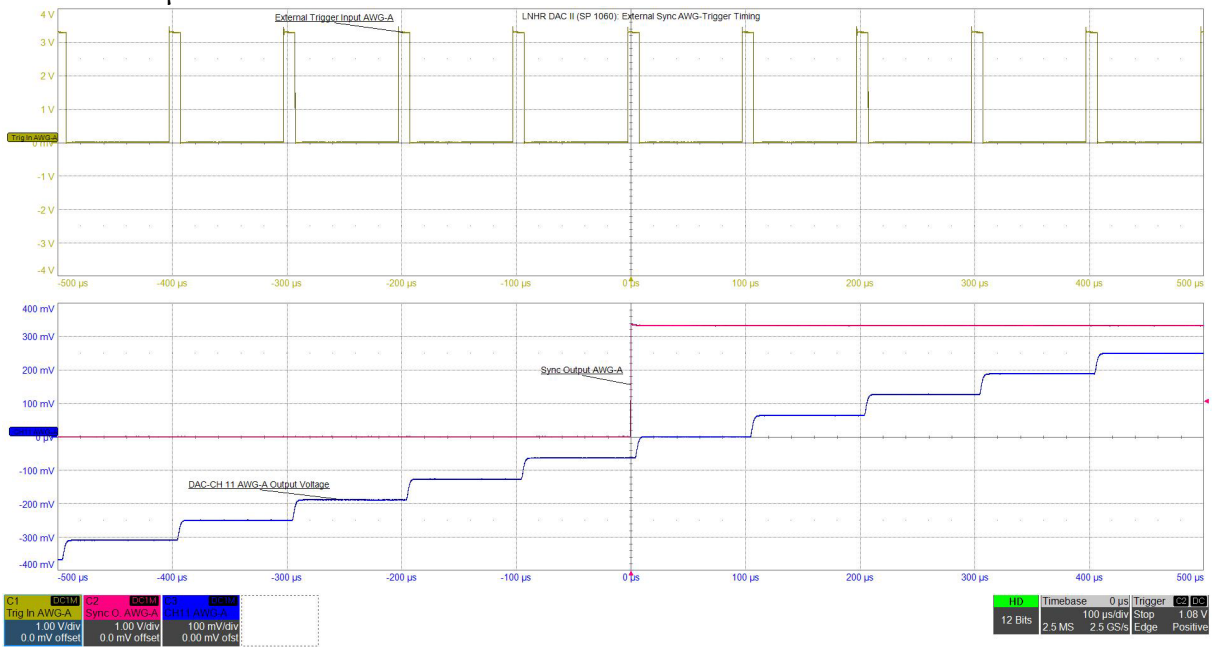
Since the AWG is stopped in the first half of the AGW-points the “Sync Out AWG-A” output signal is also truncated to a length of 400 µsec.

An infinite running AWG (AWG Cycles = 0) can be externally stopped with a falling-edge on the signal “Trig In AWG”:



The falling-edge on the “Trig In AWG” input signal immediately stops the infinite repetitive running AWG. The rising-edge has no impact, since the AWG is already started.

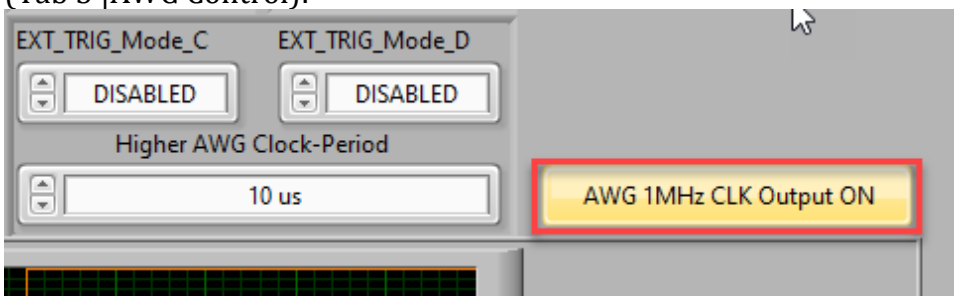
The timing in the “SINGLE-STEP” mode (same AWG values as before) with an external AWG clock-signal (applied on “Trig In AWG-A”) with a frequency of 10 kHz and a pulse-width of 10 µsec is shown below:



With each rising edge of the “Trig In AWG” input, the sinusoidal signal (predefined in AWG-A) is switched by one step. The time delay from the rising-edge of the external “Trig In AWG” input to the update of the DAC voltage is typical 6.3 µsec and the time-jitter is about 1 µsec.
In the “SINGLE-STEP” mode the user can update the AWG on the rising edge of its own external clock signal; the frequency ranges from DC up to 100 kHz with a minimum pulse-width of 2 µsec.

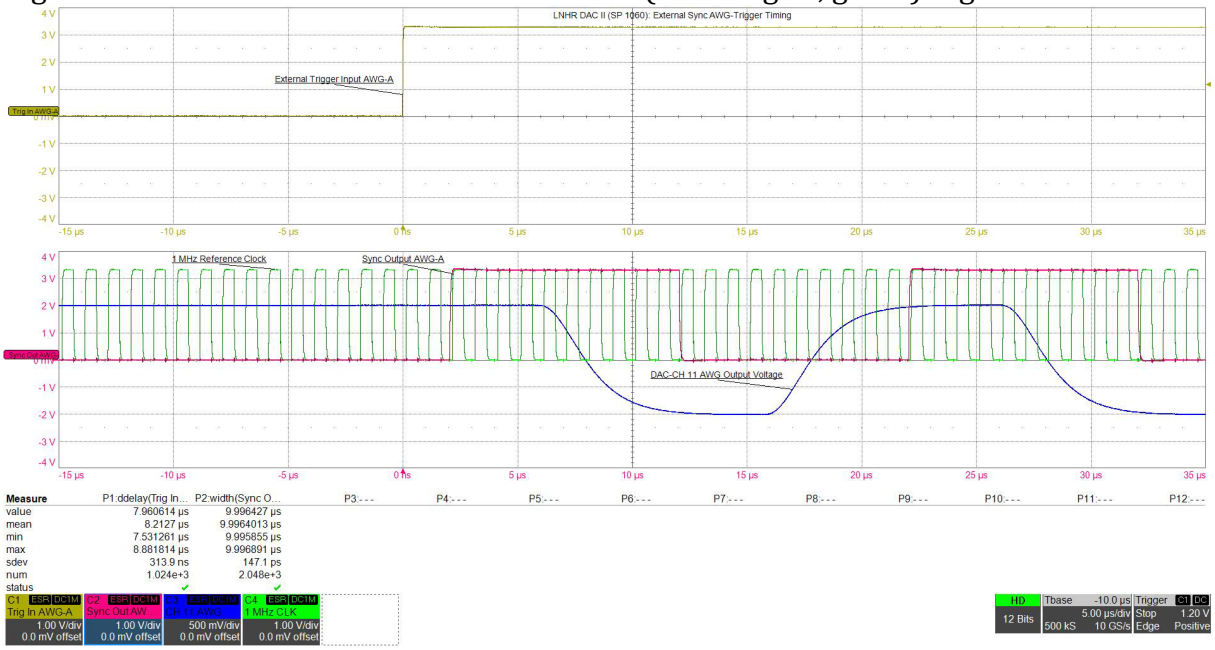
10.5.3 AWG 1 MHz Reference Clock Output

The AWG 1 MHz Reference Clock output signal can be used for time-synchronization with other devices. It is only available on pin 14 of the D-SUB 25-pin connector and is switched OFF by default to minimize the power consumption and the crosstalk to the other digital signals on the same connector. The AWG 1 MHz Reference Clock output can be switched ON via a remote command or by using the "LNHR DAC II Commander" application (Tab 3 |AWG Control):



When time-synchronization has to be done, the AWG time-jitter can be reduced by switching to the "AWG Only" mode where the DAC-Board is exclusively working for the AWG function. Then all other DAC-Channels are blocked, and its last DAC voltages are frozen and they cannot be updated. The "AWG Only" mode can be set by a remote command or by using the "LNHR DAC II Commander" application (Tab 3 | AWG Control):

The AWG 1 MHz Reference Clock is internally used for the clock generation of the four AWGs running on LNHR DAC II. The maximum AWG clock frequency is 100 kHz corresponding to an update period of 10 µsec. Below the typical AWG start timing together with the AWG 1 MHz Reference Clock (bottom grid, green) is given:



In this example the AWG function holds only two points at the two DAC voltages of ±1 V (blue). The AWG clock frequency is set to its maximum frequency of 100 kHz. The number of AWG cycles is set to two (2). The rising edge of "Trig In AWG-A" starts the two cycles which last for 40 µsec – on the printout only the first cycle is fully visible. One can identify the typical time delay of around 6.3 µsec from the rising-edge of the external "Trig In AWG-A" to the first AWG-A point converted to a DAC voltage (first step from +1 V to -1 V).

Since this AWG function is a square wave with an amplitude of ±1 V and a frequency of a 50 kHz, while the bandwidth of the DAC output is limited to 100 kHz (rise-time 3.5 µsec), the edges of the measured DAC output voltage (blue) are rounded. In the "AWG Only" mode the typical time-jitter is around 1 µsec.

11 Output Voltage Noise

In the LBW mode (100 Hz) the output voltage noise is typically 500 nV_{RMS} (3.3 μV_{PP}) measured in a frequency range of 0.1 Hz to 100 Hz and at the maximum DAC voltages of ±10 V. With smaller DAC voltages the noise voltage decreases and reaches at a DAC voltage of zero (0 V) typically 300 nV_{RMS} (2 μV_{PP}). In the LBW mode (100 Hz) most of the noise voltage is generated in the low-frequency band between 0.1 Hz and 10 Hz; this is due to the 1/f-noise.

In the HBW mode (100 kHz) the output voltage noise is typically 4 μV_{RMS} (26.4 μV_{PP}) measured in a frequency range of 0.1 Hz to 100 kHz. It is almost independent on the actual DAC voltage. For frequencies lager than 1 kHz a white voltage noise density of around 12 nV/sqrt(Hz) is reached.

The RMS noise voltage (V_{RMS}) correspond to the standard-deviation (sigma) of the gaussian normal distribution while the peak-to-peak noise voltage (V_{PP}) is estimated by applying a noise-crest factor of 6.6 (99.9 % are within this value).

The output noise voltage is measured by attaching the AC-coupled (0.03 Hz) "Low Noise / Low Drift Differential Amplifier (SP 1004)" directly to DAC voltage output. The output of the amplifier is fed to the oscilloscope via a high-pass filter with a cut-off frequency of 0.023 Hz. Below is a photo of the measurement setup:

The trace CH1 on the oscilloscope (Teledyne/LeCroy, WaveRunner 8108HD) is set to infinite persistence and the histogram of the measured voltage is calculated. Further the voltage noise density spectrum in V/sqrt(Hz) is calculated by using the FFT function. By integrating this voltage noise density spectrum, the total voltage noise (V_{RMS}) is calculated.

For such noise measurements, it is important to have a clean measurement setup in a quiet environment with no mechanical vibrations on the LNHR DAC II and on the voltage amplifier. Further the LNHR DAC II with the amplifier must be well separated from power lines and other devices generating electromagnetic AC-fields.

The noise measurement below is taken at LBW (100 Hz) and at a DAC output voltage of -10V. The voltage amplifier is set to a gain of 10'000 and has a bandwidth of 3 kHz:

The top grid shows the time domain with 1 sec/div in the horizontal axis and 1 µV/div (10 mV divided by 10'000) in the vertical axis; further the histogram (light blue) of 106 runs with 1 µV/div (10 mV divided by 10'000) in the horizontal axis is shown. The accumulation of the 106 runs takes around 17 minutes.

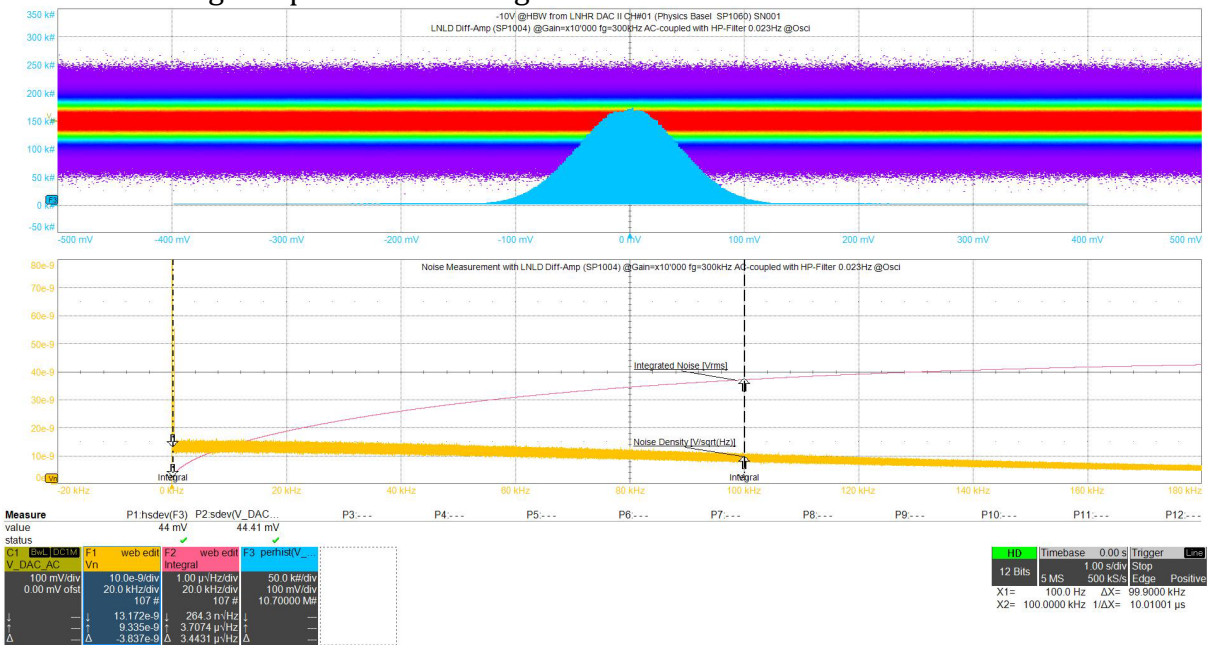
The bottom grid shows the frequency domain with 100 Hz/div in the horizontal axis and 10 nV/sqrt(Hz) for the "Noise Density Spectrum (yellow)" respective 50 nV_{RMS}/div for the "Integrated Noise Curve (red)"; for both traces the average of the 106 runs is taken.

For this specific measurement, the integrated noise from 0.1 Hz to 10 Hz is about 200 nV_{RMS} and from 0.1 Hz to 100 Hz around 240 nV_{RMS}; this is even better than the typical 500 nV_{RMS} specified above. On the "Noise Density Spectrum (yellow)" the European mains-frequency of 50 Hz and some of its harmonics can be clearly identified. As seen on the "Integrated Noise Curve (red)" those peaks do not add significant to the total noise voltage (V_{RMS}).

For frequencies above 100 Hz the "Noise Density Spectrum (yellow)" drops due to 100 Hz LP-filter (LBW) and reaches at 900 Hz almost the noise floor of 1 nV/sqrt(Hz), coming from the voltage amplifier (SP 1004).

The total integrated noise from 0.1 Hz to 900 Hz is around 280 nV_{RMS} which is compatible with the measured standard deviation of the histogram (light blue) of around 310 nV_{RMS} (3.1 mV divided by 10'000). The difference comes from the fact that the "Noise Density Spectrum (yellow)" starts at 0.1 Hz (given by the FFT), while the histogram holds frequencies down to around 0.04 Hz which is given from system high-pass cut-off frequency. Due to the 1/f-noise, the lower cut-off frequency of the histogram leads to a slightly higher measured noise in V_{RMS} (standard-deviation).

The noise measurement below is taken at HBW (100 kHz) and at a DAC output voltage of -10V. The voltage amplifier is set to a gain of 10'000 and has a bandwidth of 300 kHz:



The top grid shows the time domain with 1 sec/div in the horizontal axis and 10 µV/div (100 mV divided by 10'000) in the vertical axis; further the histogram (light blue) of 107 runs with 10 µV/div (100 mV divided by 10'000) in the horizontal axis is shown. The accumulation of the 107 runs takes around 17 minutes.

The bottom grid shows the frequency domain with 20 kHz/div in the horizontal axis and 10 nV/sqrt(Hz) for the "Noise Density Spectrum (yellow)" respective 1 μV_{RMS}/div for the "Integrated Noise Curve (red)" in the vertical axis; for both traces the average of the 107 runs is taken.

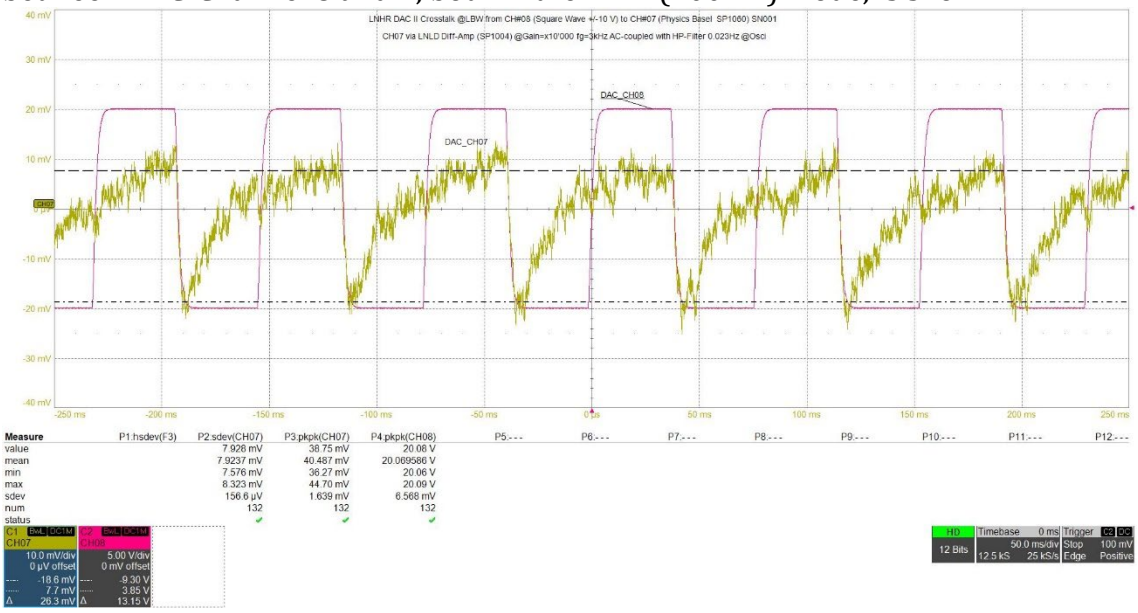
For this specific measurement, the integrated noise from 0.1 Hz to 100 Hz is about 264 nV_{RMS} and from 0.1 Hz to 100 kHz around 3.7 μV_{RMS}; this is even better than the typical 4 μV_{RMS} specified above.

The "Noise Density Spectrum (yellow)" shows no noise-peaks at higher frequencies and one can see that the white noise density of around 12 nV/sqrt(Hz) is reached for frequencies higher than 1 kHz.

For frequencies above 100 kHz the "Noise Density Spectrum (yellow)" drops due to the 100 kHz LP-filter (HBW). The total integrated noise from 0.1 Hz to 180 kHz is around 4.3 μV_{RMS} which is compatible with the measured standard deviation of the histogram (light blue) of around 4.4 μV_{RMS} (44 mV divided by 10'000).

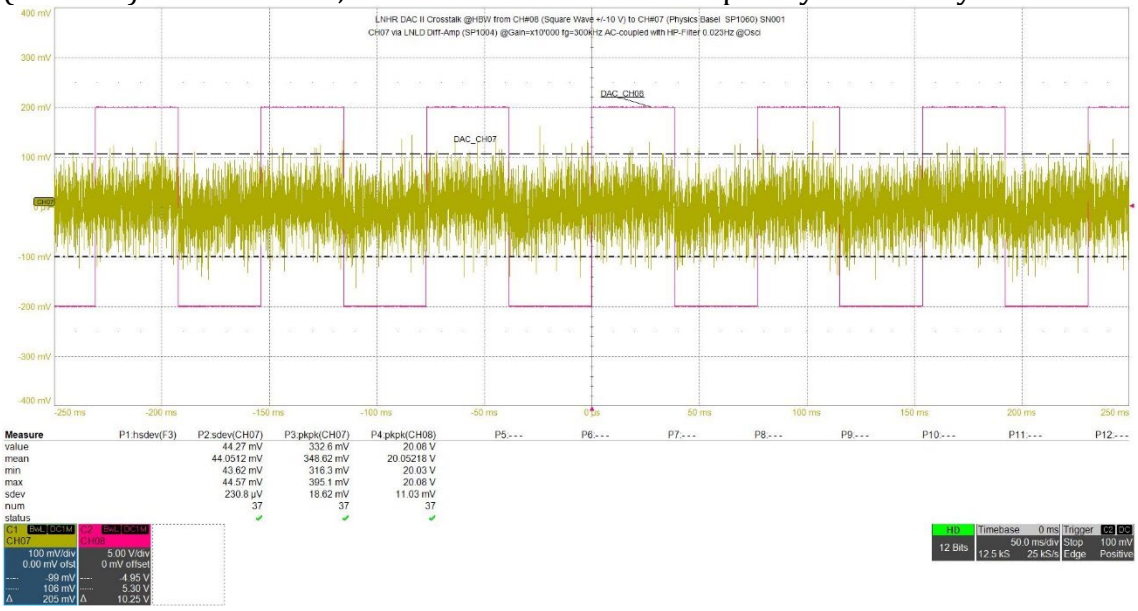
12 Crosstalk Isolation

The crosstalk isolation can be measured with the same setup as for the noise measurement; this number shows how well a DAC channel is isolated from its neighboring DAC channel. Measurements show that only in the LBW (100 Hz) mode the crosstalk can be clearly identified at all because of the noise. In the HBW (100 kHz) mode the crosstalk is almost completely covered by the noise. Below the crosstalk isolation measurement between DAC-Channel 8 and 7, both in the LBW (100 Hz) mode, is shown:



On the DAC-Channel 8 a square wave with an amplitude of 20 V_{pp} (±10 V) and frequency of 13 Hz is generated by using the AWG function. On the adjacent DAC-Channel 7 the crosstalk residual signal is measured by using the AC-coupled (0.03 Hz) "Low Noise / Low Drift Differential Amplifier (SP 1004)" with a gain of 10'000. The residual peak to peak signal is around 2.63 μV_{pp} (26.3 mV_{pp} / 10'000). This corresponds to crosstalk isolation of 137.6 dB; this was the highest residual signal found on many different channel combinations. Therefore, a <u>crosstalk isolation of larger than 137 dB is specified</u>.

Below the same crosstalk isolation measurement with both DAC-Channels in the HBW (100 kHz) mode is taken; the crosstalk is almost completely covered by the noise:



13 Temperature Drift

The temperature drifts of the DAC output voltages were measured in a precise temperature-controlled chamber by changing the ambient temperature from 10°C to 40°C in 5°C steps. The measurements were performed at different DAC voltages (0 V / ±5 V / ±10 V) and in LBW (100 Hz) as well as in HBW (100 kHz) mode. It turned out that the measured voltage drift is dependent on the DAC voltage, but independent of the selected bandwidth (LBW or HBW).

Within an ambient temperature range of 10 °C to 40 °C:
The following typical voltage drift (dV [V]) at a nominal DAC voltage (V_{DAC} [V]) due to a change in ambient temperature (dT [K]) was determined:

$$dV = dT * (C_1 + C_2 * V_{DAC})$$

C_1 = 1 µV/K (independent of the DAC voltage)
C_2 = 1.5 ppm/K (dependent on the DAC voltage)

By applying these parameters, the typical voltage drift (dV [V]) at a nominal DAC voltage (V_{DAC} [V]) due to a change in ambient temperature (dT [K]) can be calculated by the following equation:

$$dV = dT * (1\ \mu V/K + 1.5\ ppm/K * V_{DAC})$$

Example:
Nominal DAC voltage: 5.000000 V
Change in ambient temperature: 10°C => 10 K

dV = 10 * (1 µV + 1.5E-6 * 5 V) = $85\ \mu V$

This means that a nominal DAC voltage of 5.000000 V will drift by typical 85 µV when the temperature changes by 10°C (10 K). Since the sign of the dV/dT is unknown, the DAC voltage can be in a range from 5.000085 V to 4.999915 V after the ambient temperature has changed by 10 °C.

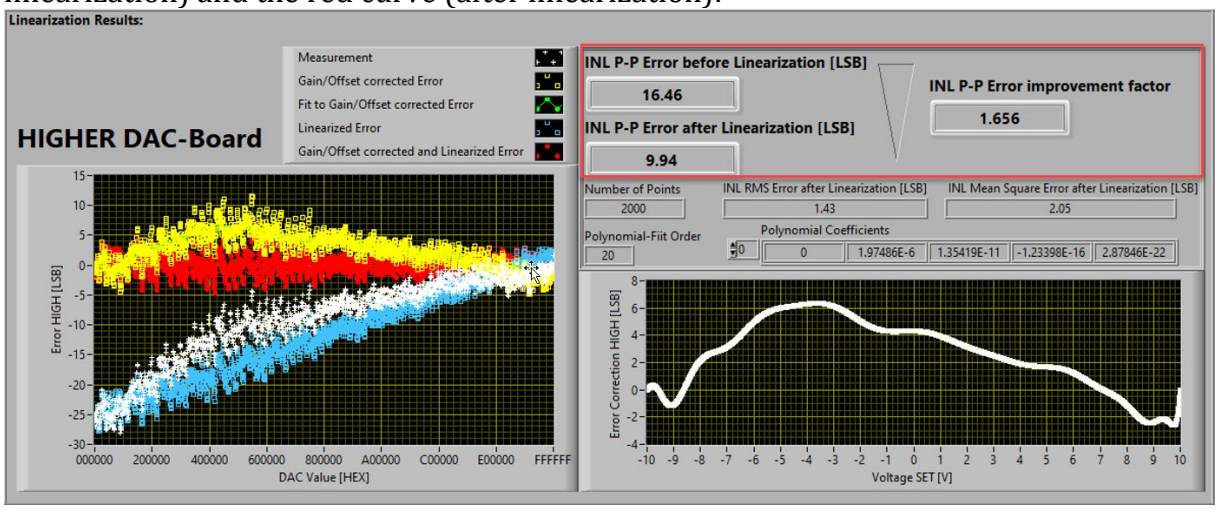
14 Nonlinearity (INL)

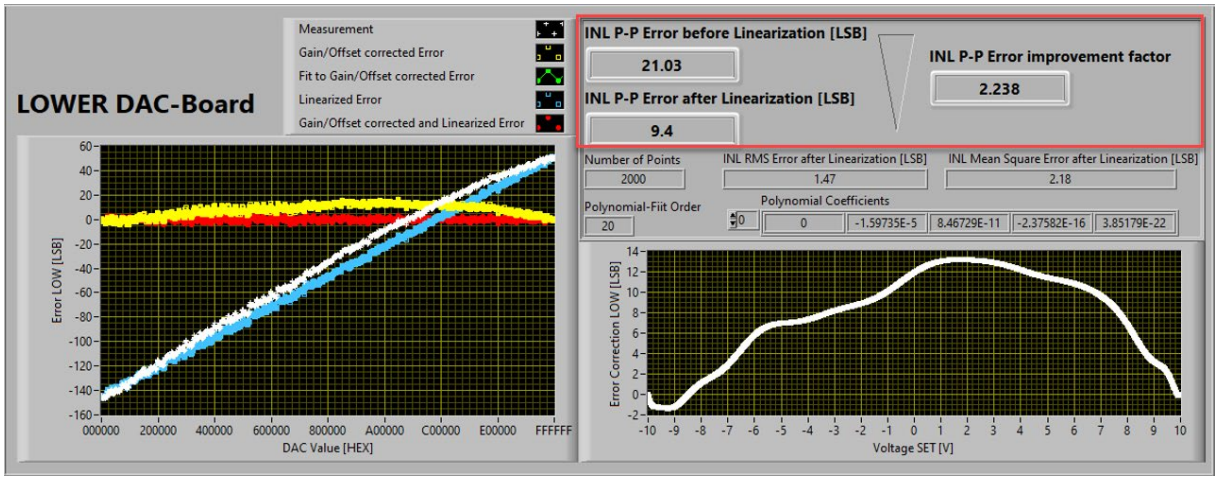
After production, each DAC-Channel of the LNHR DAC II is linearize in a complex calibration process. The DAC voltage is finely varied over its entire -10V to +10V range while the output voltage is measured and registered with a high-precision reference multimeter (Fluke 8588A). From these measurements the linearization polynomial error coefficients are calculated by a polynomial-fit (20th order). By applying this polynomial error correction, the 24-bit DAC gets linearized with respect to the reference multimeter.

For every DAC value written this linearization is immediately applied "on the fly". The linearization coefficients of all the DAC-Channels are stored on the LNHR DAC II and they are read into the memory when the device is started.

With this individual linearization a typical INL (Integral Nonlinearity) of only ±7 LSB can be reached. This corresponds to a typical integral nonlinearity voltage-error of ±8.4 µV over the entire DAC range from -10 V to +10 V.

Below the linearization results of two typical DAC-Channels are shown. In the graph on the left you can see the linearity improvement by comparing the yellow curve (before linearization) and the red curve (after linearization):





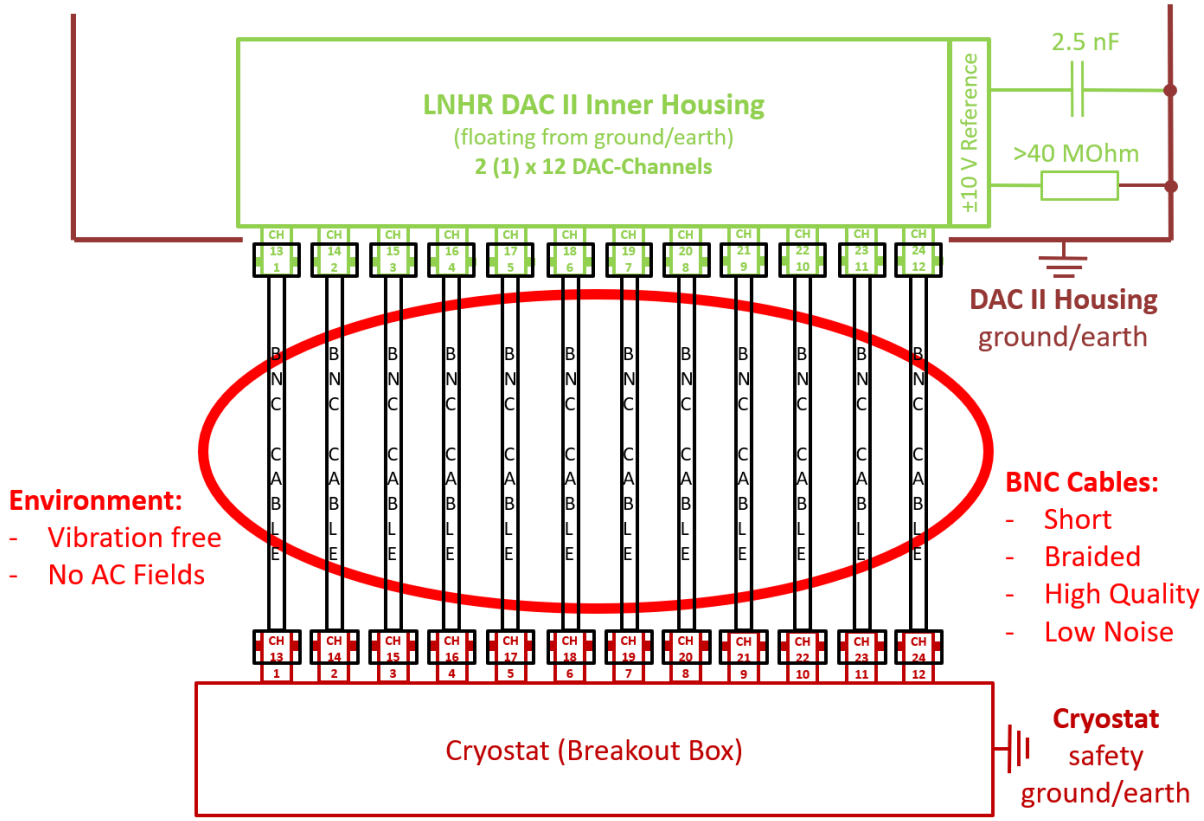
After the linearization procedure the residual "INL P-P Error" for both DAC-Channels are below 10 LSB which corresponds to an INL of only ±5 LSB. By applying this linearization process, the INL can typically be improved by a factor of two.

15 Grounding and Wiring

Grounding and wiring are also very important to ensure the high quality and low noise performance of the DAC voltages up to the cryostat.

The most important thing is to avoid a ground loop between the cryostat and the DAC voltage source. Normally, the cryostat is grounded to a safety grounded/earth coming from the magnet power-supplies. To break the ground loop, the DAC II outputs are isolated from the housing/earth. This is achieved by installing the DAC-Channels in galvanically isolated "Inner Housing", which is floating from ground/earth. All the DAC-Channels are referenced to the same ground (AGND) which can be floating by maximum ±20 V with respect to the ground/earth.

Via the shields of the BNC cables, the "Inner Housing" of the LNHR DAC II gets referenced to the safety grounded/earth of the cryostat and no (or only very small) ground loop current can flow. The coupling impedance between the "Inner Housing" (AGND) and the outer housing (ground/earth) is typical >40 Mega Ohm in parallel with a capacitance of only around 2.5 nF. This small coupling capacitance results also in very small AC ground loop currents, even at higher frequencies. The block diagram below shows the typical grounding and wiring between the cryostat and the LNHR DAC II:



Wiring the DAC outputs to the cryostat should be done by using high quality and low vibration-noise coaxial BNC cables (e.g. Huber & Suhner G_03130_HT). The cable length should be as short as possible and they must be kept away from sources of mechanical vibration or electrical AC fields. Further, the coaxial cables should be braided together to minimize the open coupling area for AC stray magnetic fields.

16 Converting DAC-Voltage to DAC-Value

A DAC-Value is a 24-bit number in the decimal range from 0 to 16'777'215 (2^{24}-1); this corresponds to a hexadecimal range from 0x000000 to 0xFFFFFF.

The DAC-Voltage has a fixed range from -10 V to +10 V with a step-size of 1.192093 µV (20 V / 16'777'215).

For a given DAC output voltage (Vout [-10 V ...+10 V]) the 24-bit decimal DAC-Value (DACval [0…16'777'215]=[0x000000…0xFFFFFF]) is given by (rounded to the next integer value):

$$DACval\_dec = (Vout + 10) \cdot 838'860.74$$

To get a DAC-Value (HEX), which is needed for remote programming the DAC output voltage, the decimal number has to be converted to a hexadecimal number. All higher program languages have already included such a conversion-function.

For a given decimal DAC-Value (DACval_dec [0...16'777'215]=[0x000000…0xFFFFFF]) the DAC output voltage (Vout [-10 V...+10 V]) can be determined by:

$$Vout = (DACval\_dec / 838'860.74) - 10$$

The table below shows the DAC-Voltage [±10 V] in 1 V steps and the calculated DAC-Value (decimal) and the corresponding DAC-Value (HEX):

DAC-Voltage	DAC-Value (decimal)	DAC-Value (HEX)
+10 V	16'777'215	0xFFFFFF
+9 V	15'938'354	0xF33332
+8 V	15'099'493	0xE66665
+7 V	14'260'633	0xD99999
+6 V	13'421'772	0xCCCCCC
+5 V	12'582'911	0xBFFFFF
+4 V	11'744'050	0xB33332
+3 V	10'905'190	0xA66666
+2 V	10'066'329	0x999999
+1 V	9'227'468	0x8CCCCC
0 V	8'388'607	0x7FFFFF
-1 V	7'549'747	0x733333
-2 V	6'710'886	0x666666
-3 V	5'872'025	0x599999
-4 V	5'033'164	0x4CCCCC
-5 V	4'194'304	0x400000
-6 V	3'355'443	0x333333
-7 V	2'516'582	0x266666
-8 V	1'677'721	0x199999
-9 V	838'861	0x0CCCCD
-10 V	0	0x000000

17 Specifications (Typical @Temperature 25°C, 2 h Warm-up)

- Number of DAC-Channels: 24 or 12
- BNC connector spacing: 25 mm horizontal, 21.6 mm vertical (24 DAC-Channels)
- DAC output voltage range: ±10 V
- Absolute DAC output voltage accuracy (over the entire ±10 V): ±200 µV
- Resolution: 24-bit (1.2 µV step size), independent of selected bandwidth
- Bandwidth: 100 Hz (LBW) or 100 kHz (HBW) – individual selectable
- Total integrated output voltage noise:
  LBW @V_{DAC} = 0 V (0.1 Hz…100 Hz): 300 nV_{RMS}
  LBW @V_{DAC} = ±10 V (0.1 Hz…100 Hz): 500 nV_{RMS}
  HBW @V_{DAC} = 0V… ±10 V (0.1 Hz…100 kHz): 4 μV_{RMS}
- Voltage noise density @HBW (f > 1 kHz): 12 nV/sqrt(Hz)
- Rise-time (10% to 90%):
  LBW (100 Hz): 3.5 msec
  HBW (100 kHz): 3.5 µsec
- Temperature drift: 1 µV/K + 1.5 ppm/K (from actual DAC voltage)
- Integral Nonlinearity (INL): ±7 LSB (corresponds to ±8.4 µV over ±10 V)
- ON state output: Actively driven with a 50 Ohm impedance
- OFF state output: Passively grounded via 1 Mega Ohm // 22 nF
- DAC voltage decay-time @OFF state: 48 msec (90% to 10%)
- Output current: 1 mA on all DAC-Channels /10 mA on one DAC-Channel per board
- Channel to channel crosstalk isolation: >137 dB
- DAC output ground AGND: Isolated from housing and computer interface
- Voltage between AGND and housing (ground/earth): maximum ±20 V
- Coupling between AGND and housing (ground/earth): >40 MegOhm // 2.5 nF
- Warm-up time: 2 hours
- Supply voltage: 24V_{DC} ±10%
- Power consumption (24 DAC-Channels): Typ. 24 W / Max. 36 W (24 V_{DC}, 1.5 A)
- Power supply: Wall plug 24 V_{DC} / 1.66 A, MeanWell GEM40I24 (included)
- Power supply cable length: 3 meters
- System startup time: 45 sec
- Local display: 4 x 20 dot-matrix LCD, 4.75mm character-height
- Ethernet port speed: 10 or 100 or 1000 Mbit/sec
- RS-232 Baud rate: 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bit/sec
- Housing: 19" desktop and rack mount (2U height)
- Housing dimensions: Width 480 mm, Height 100 mm, Depth 350 mm
- Weight, including the power supply: 7.7 kg (17 lb.)

18 Operation Conditions

- Environment: Indoors dry laboratories only
- Ambient Temperature: Between 10°C (50°F) and 40°C (104°F)
- Altitude: Up to 5'000 m (16'400 ft)
- Maximum relative humidity: Maximum 90% for temperatures up to 31°C (88°F), decreases linearly tom 50% at 40°C (104°F)
- Pollution: Degree 1 (no pollution or only dry and non-conductive pollution)

19 Table of Content

Notes: